JVC

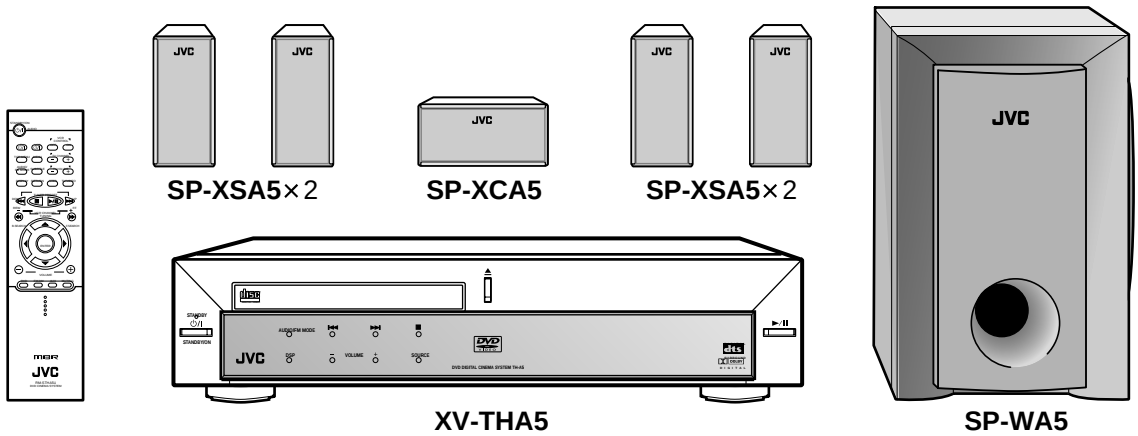
SERVICE MANUAL

DVD DIGITAL CINEMA SYSTEM

TH-A5

Area suffix

A ---------- Australia
US ---------- Singapore
UB ---------- Hong Kong
UW -- Brazil,Mexico,Peru
UY ---------- Argentina
UJ ---------- U.S.Military
UG ---------- Turkey, South Africa,Egypt

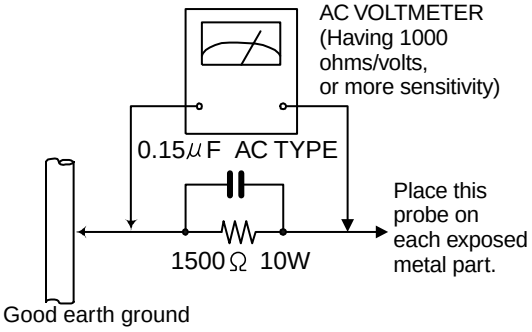


Contents

No.21062
Jan. 2002

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ CAUTION

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▮) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.

(This regulation does not correspond to J and C version.)

Important for laser products

1.CLASS 1 LASER PRODUCT

2.DANGER : Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.

3.CAUTION : There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

4.CAUTION : The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.

5.CAUTION : If safety switches malfunction, the laser is able to function.

6.CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠ ***CAUTION*** **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

REPRODUCTION AND POSITION OF LABELS

Preventing static electricity

1.Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

2.About the earth processing for the destruction prevention by static electricity

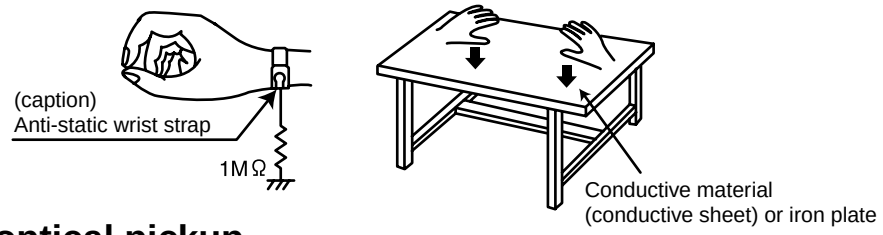
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players. Be careful to use proper grounding in the area where repairs are being performed.

2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

4.Handling the traverse unit (optical pickup)

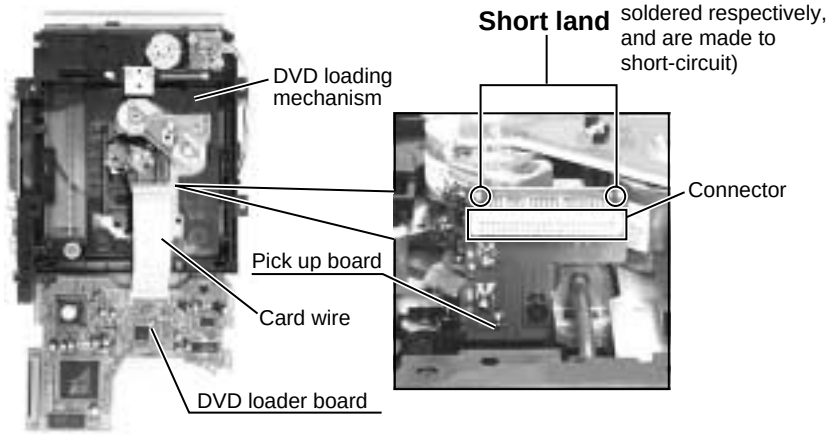
1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
3. Handle the flexible cable carefully as it may break when subjected to strong force.
4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it.

Attention when traverse unit is decomposed

***Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.**

1. Solder is put up before the card wire is removed from connector on the pick up board as shown in Figure.
   (When the wire is removed without putting up solder, the CD pick-up assembly might destroy.)
2. Please remove solder after connecting the card wire with when you install picking up in the substrate.

DVD mechanism assembly (bottom side)



Disassembly method

■Removing the top cover (See Fig.1)

1. Remove the four screws **A** attaching the top cover on the both sides of the body.

2. Remove the two screws **B** on the back of the body.

3. Remove the top cover from behind in the direction of the arrow while pulling both sides outward.

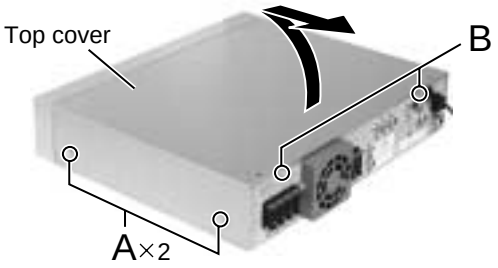


Fig.1

■Removing the front panel assembly (See Fig.2A, 2B and 3)

- Prior to performing the following procedure, remove the top cover.

1. Remove the one screw **a** and remove the earth wier.

2. Remove the three screws **C** attaching the front panel assembly on the bottom of the body.

3. Remove the two screws **D** attaching the front panel assembly on the both sides of the body.

4. Remove the claw1, claw2 and claw3, and detach the front panel assembly toward the front.

5. Disconnect the card wire from the connector DW20 on the DSP board.

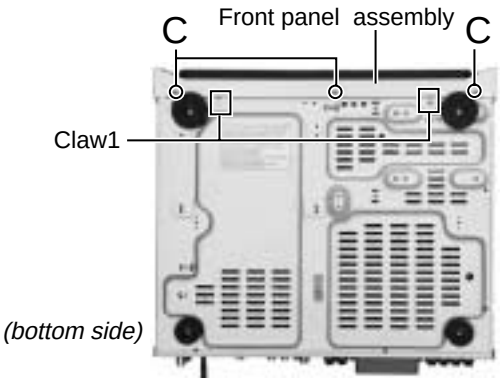


Fig.2A

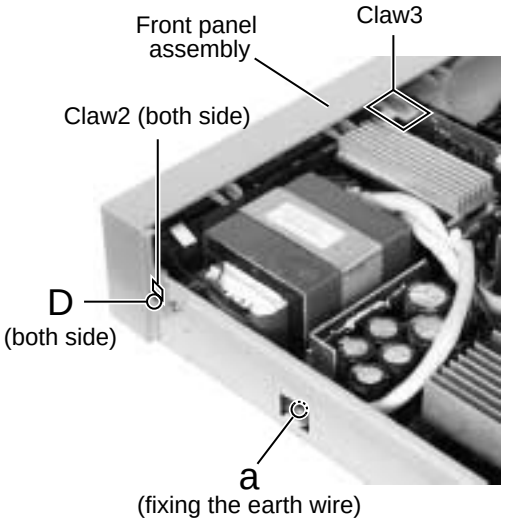


Fig.2B

■Removing the power cord (See Fig.4)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the power cord from the connector CW1 on the main board and pull up the cord stopper upward.

Notes : The power cord is exchangeable.

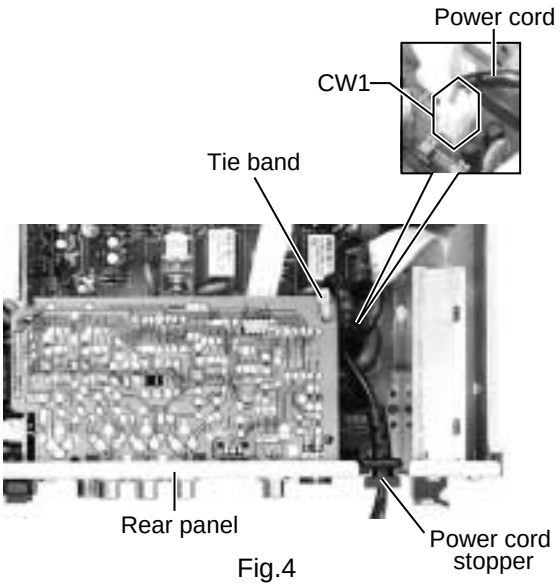


Fig.4

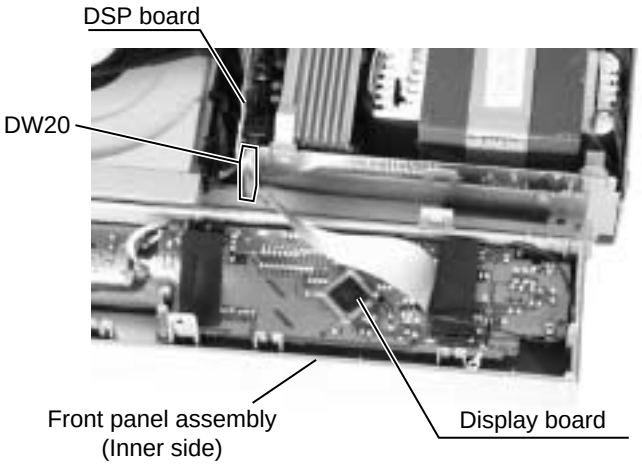


Fig.3

■Removing the DVD mechanism assembly (See Fig.5 and 6)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from the connector J14 and J21 on the DVD MPEG board.
2. Remove the two screws **E** attaching the DVD mechanism assembly and pull up with drawing out.
3. Disconnect the harness from the connector J2 on the DVD loader board.

■Removing the rear panel (See Fig.7 and 8)

- Prior to performing the following procedure, remove the top cover and power cord.

1. Disconnect the harness from the connector NW11 on the DSP board.
2. Remove the two screws **F**, four screws **G**, five screws **I** attaching the each boards to the rear panel.
3. Remove the three screws **J** attaching the rear panel on the back of the body.

■Removing the tuner pack (See Fig.7 and 8)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from the connector CON01 on the tuner pack.
2. Remove the two screws **F** attaching the tuner pack to the rear panel.

■Removing the jack board (See Fig.7 and 8)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from the connector VW2 on the jack board.
2. Remove the four screws **G** attaching the jack board to the rear panel.
3. Disconnect the connector VW1 on the jack board and pull up the jack board.

■Removing the fan motor (See Fig.7 and 8)

- Prior to performing the following procedures, remove the top cover .

1. Disconnect the harness from the connector NW11 on the DSP board .
2. Removing the two screws **H** attaching the fan motor on the rear panel.

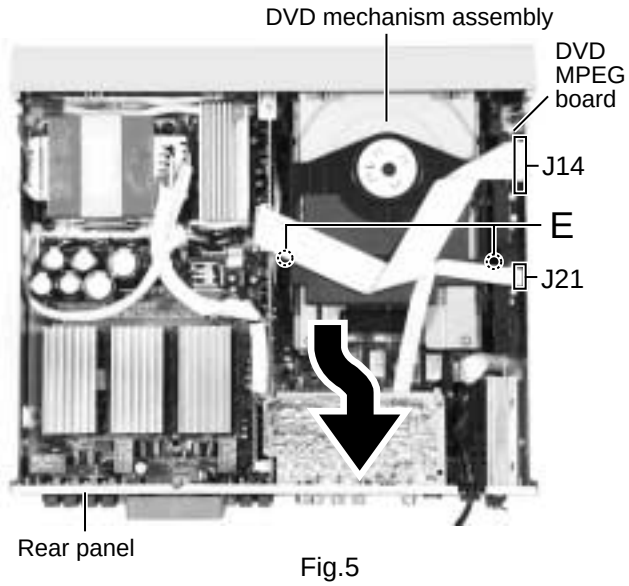


Fig.5

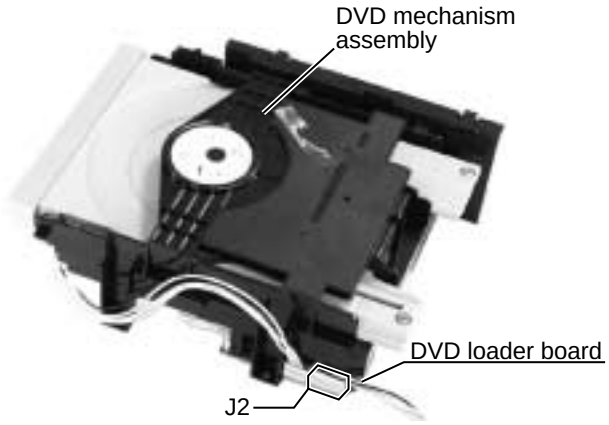


Fig.6

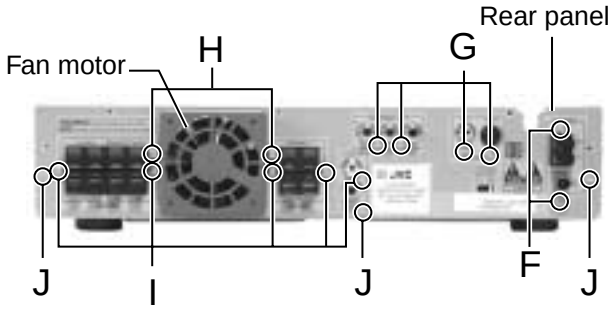


Fig.7

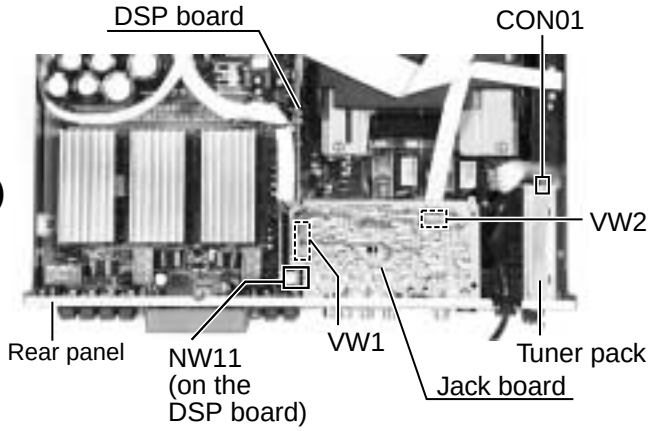


Fig.8

■ Removing the DSP board (See Fig.9)

・Prior to performing the following procedure, remove the top cover, the front panel assembly and jack board.

1. Untied the harness band and disconnect the harness from the connector CW2 on the main board.
2. Disconnect the harness from the connector NW11 on the DSP board.
3. Disconnect the card wire from the connector VW12 on the DSP board.
4. Pull up the DSP board from the front side upwards disconnecting the connector DW10, DW13, DW14 and DW15.

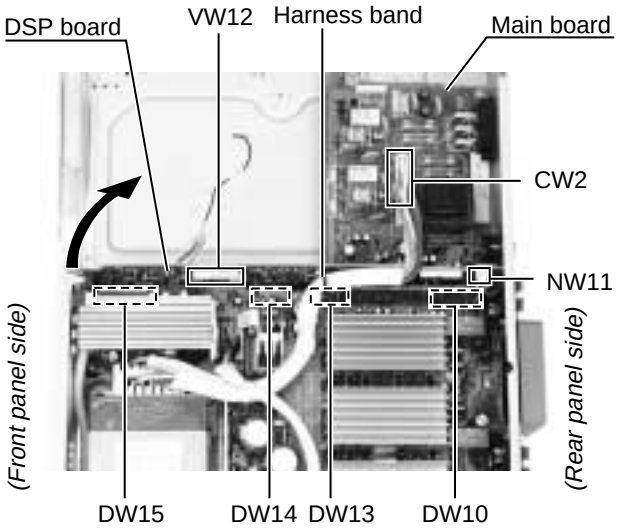


Fig.9

■ Removing the main board (See Fig.10)

・Prior to performing the following procedure, remove the top cover, front panel assembly, DVD mechanism assembly, jack board and DSP board.

1. Disconnect the card wire from the connector CW4 and CW8 on the main board.
2. Disconnect the harness from the connector CW3 on the main board.
3. Remove the five screws **I** attaching the speaker terminals and jack to the rear panel (see fig.7).
4. Remove the six screws **K1** (short) and one screw **K2** (long) attaching the main board.
5. When the rear panel is not removed, pull up the main board from front side.

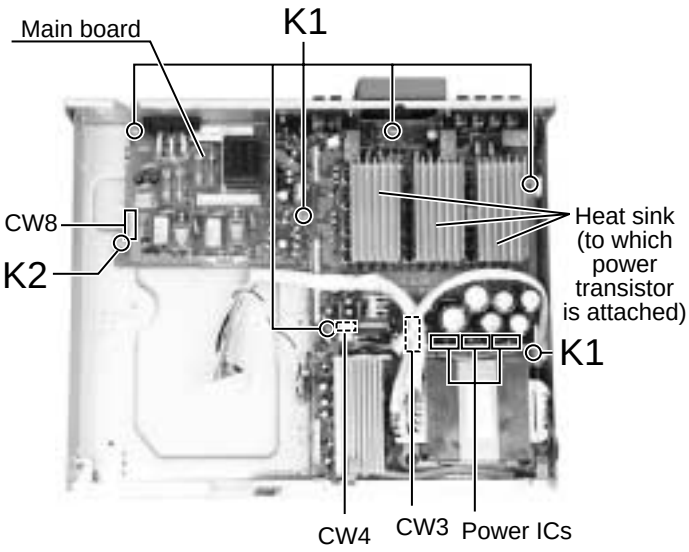


Fig.10

■ Removing the power transistor & power IC (See Fig.10 and 11)

・Prior to performing the following procedure, remove the top cover, front panel assembly, DVD mechanism assembly, jack board, DSP board and main board.

1. After removing the solder part soldered to the main board, remove each screw and remove the heat sink from Power transistor.
2. After removing the solder part soldered to the main board, remove each screw and remove the heat sink from Power IC.

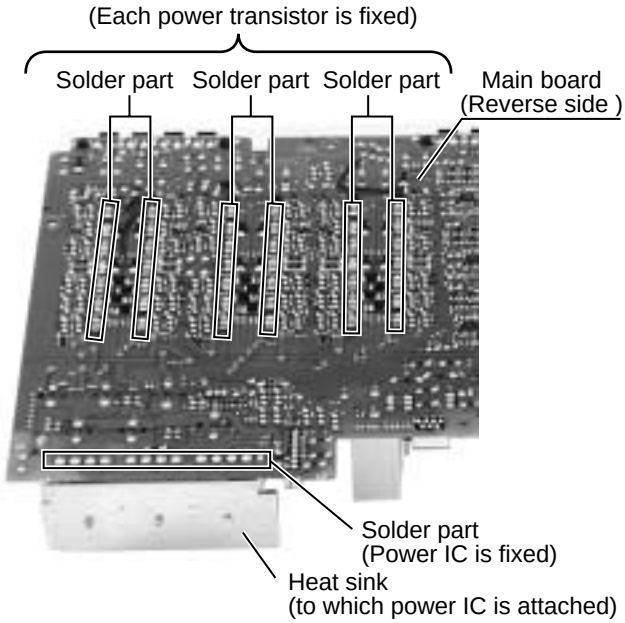


Fig.11

■ Removing the DVD power board (See Fig.12)

- Prior to performing the following procedure, remove the top cover, front panel assembly and DSP board.

1. Disconnect the harness and card wire from the connector PW1, PW2 and PW5 on the DVD power board.

2. Remove the one screw **L1** (short) and two screws **L2** (long) attaching the DVD power board.

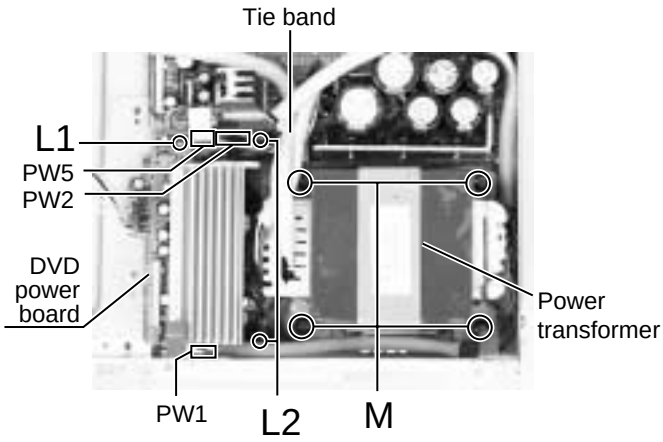


Fig.12

■ Removing the power transformer (See Fig.12)

- Prior to performing the following procedure, remove the top cover.

1. Cut off the tie band fixing the harness, if needed.

2. Disconnect the harness from the connector CW2 on the main board (see fig.9) and PW1, PW2 on the DVD power board.

3. Remove the four screws **M** attaching the power transformer.

<Front panel assembly section>

■ Removing the display board & switch board (See Fig.1 and 2)

- Prior to performing the following procedure, remove the top cover and the front panel assembly.

1. Disconnect the card wire from the connector FW1 on the display board.

2. Remove the five screws **A** attaching the display board on the inner of the front panel assembly.

3. Remove the four screws **B** attaching the switch board on the inner of the front panel assembly.

4. Disconnect the harness from connector FW2 on the display board, if needed.

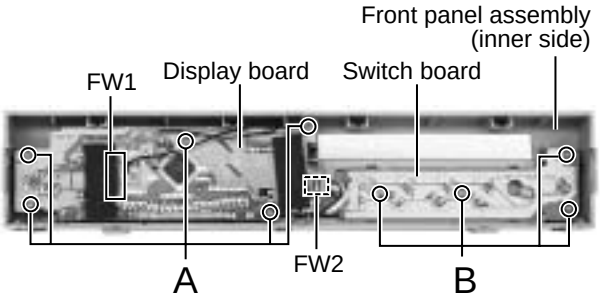


Fig.1

■ Removing the front window (See Fig.2 and 3)

- Prior to performing the following procedure, remove the top cover, front panel assembly, display board and switch board.

1. Remove the switch buttons, if needed.

2. Remove the three screws **C** attaching the front window on the front panel.

3. Remove the eight claws fixing the front window on the front panel.

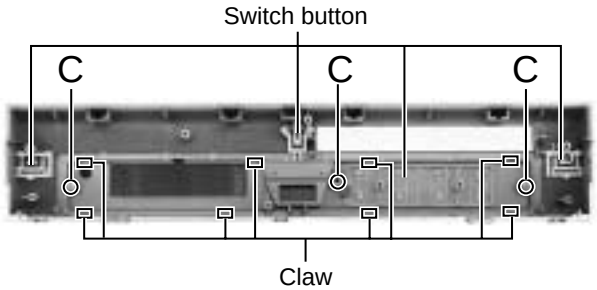


Fig.2

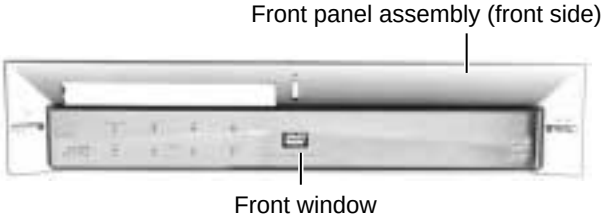


Fig.3

<DVD mechanism assembly section>

■Removing the DVD loader board (See Fig.1 to 3)

- Prior to performing the following procedure, remove the top cover and DVD mechanism assembly.

1. Disconnect the card wire from the connector J6 on the DVD MPEG board.
2. Disconnect the harness from the connector on the motor board.
3. Disconnect the harness from the connector J5 on the DVD loader board.
4. Remove the four screws **A** attaching the DVD loader board to DVD mechanism assembly.

CAUTION!! (see fig.3)

Before removing the card wire which connects the pickup board and DVD loader board, solder the two soldering parts and make it short-circuit.
Moreover, while having removed the card wire, don't remove these solder.

5. Disconnect the card wire from the connector U9 on the DVD loader board.

ONE POINT

■How to eject the DVD tray manually (see fig.2)

The white lever of the ★ mark is moved in the direction of the arrow. Then, the tray will be opened.
Moreover, the tray is separable from a DVD mechanism assembly by removing two screws of the☆mark (see fig.1) and drawing out the tray.

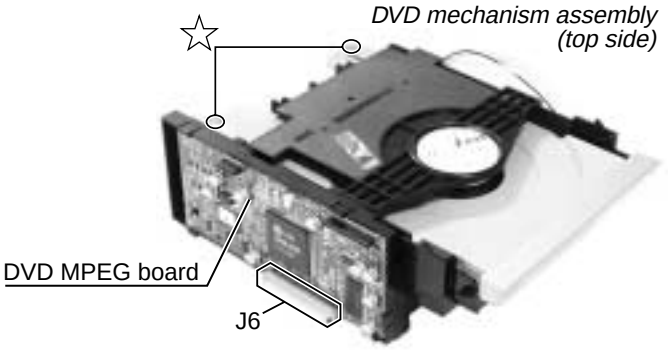


Fig.1

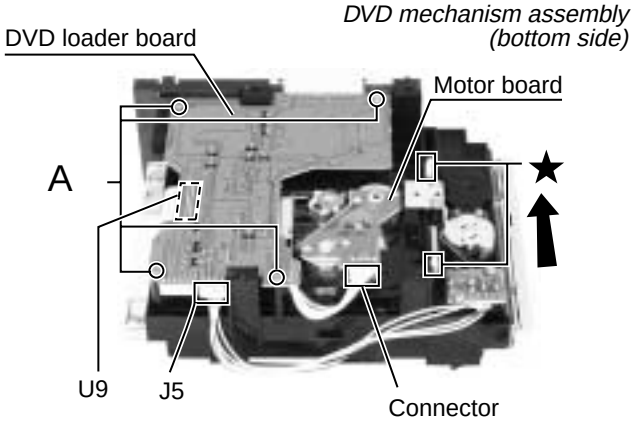


Fig.2

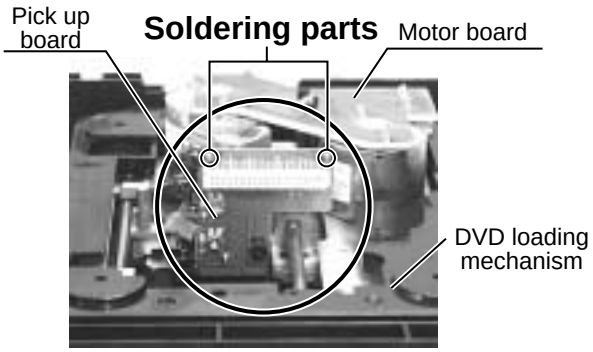


Fig.3

■Removing the DVD loading mechanism (See Fig.4)

- Prior to performing the following procedure, remove the top cover, DVD mechanism assembly and DVD loader board.

1. Remove the two screws **B** and remove the bracket.
2. Remove the one screw **C** fixing the DVD loading mechanism.
3. Move the lever in the direction of the arrow **X**.
4. Remove the DVD loading mechanism from the DVD mechanism assembly by moving it in the direction of the arrow **Y**.

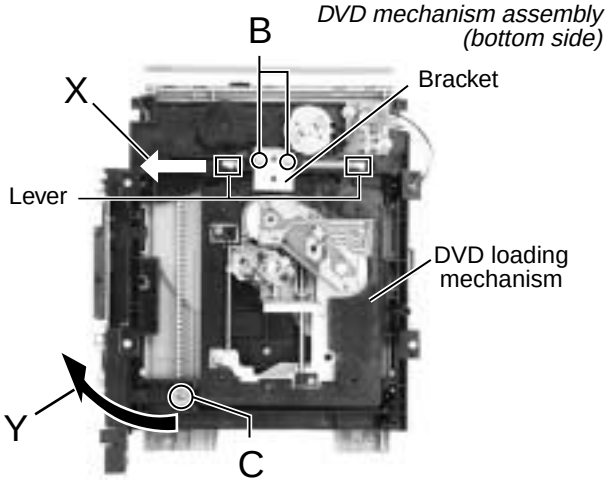


Fig.4

■Removing the DVD traverse mechanism (See Fig.5)

・Prior to performing the following procedure, remove the top cover, DVD mechanism assembly, DVD loader board and DVD loading mechanism.

1. Remove the four screws **D** attaching the DVD traverse mechanism to DVD loading mechanism.

DVD loading mechanism (top side)

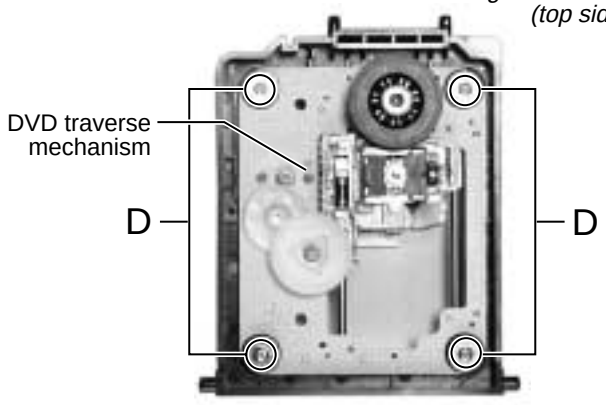


Fig.5

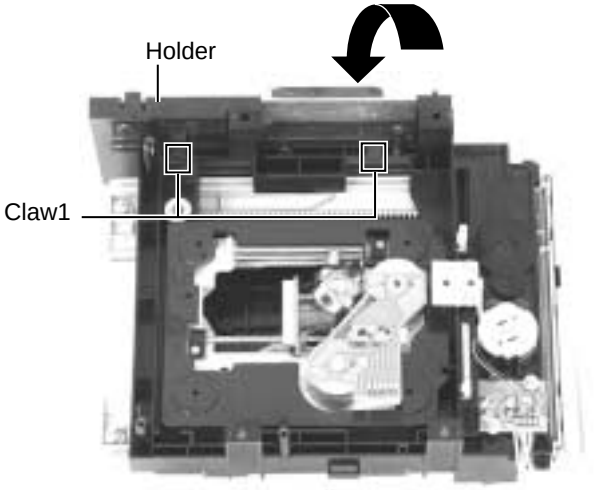
■Removing the holder & DVD MPEG board (See Fig.6 and 7)

・Prior to performing the following procedure, remove the top cover, DVD mechanism assembly and DVD loader board.

1. Remove the two claws1, and remove the holder from the DVD mechanism assembly as it is pushed down.

   Note: When removing only the DVD MPEG board, it is not necessary to remove this holder.

2. Remove the four claws2 and remove the DVD MPEG board from the holder.



DVD mechanism assembly (bottom side)

Fig.6

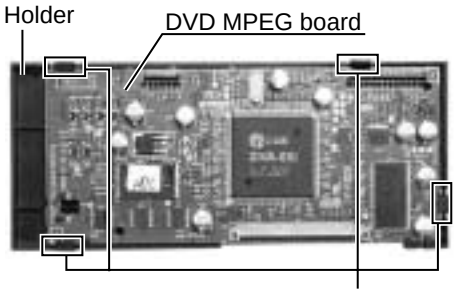


Fig.7

ONE POINT

■**When inserting DVD MPEG board in holder. (see fig.8)**

Insert in after uniting with a lower claws, when inserting DVD MPEG board in holder.

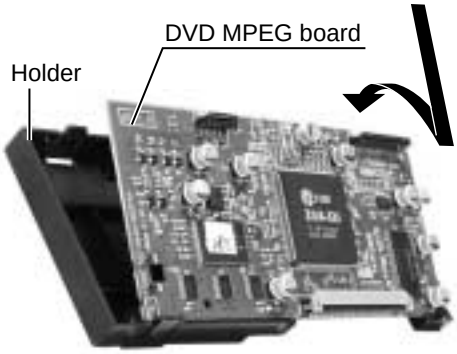


Fig.8

<Speaker section>

[SP-XSA5 / Satellite speaker]

● It is exchange in a unit.

[SP-XCA5 / Center speaker]

● It is exchange in a unit.

[SP-WA5 / Woofer]

■ Removing the front panel

(See Fig.1 and 2)

1. Remove the six bosses and remove the front panel.

   Notes: It will be good to use the tool with a flat tip, since it is hard to remove. Please take care not to damage the cabinet at this time.

2. The packing separates. It removes if needed.

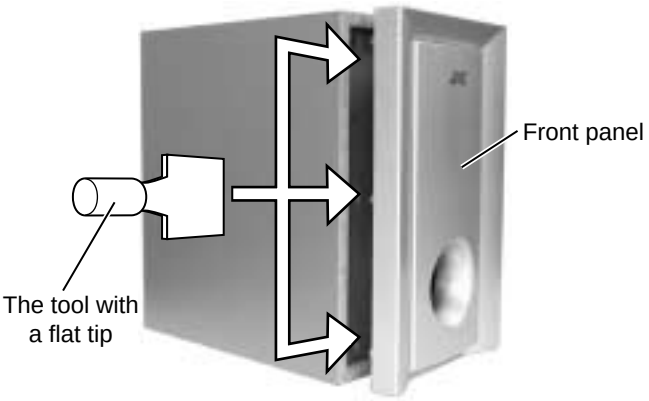


Fig.1

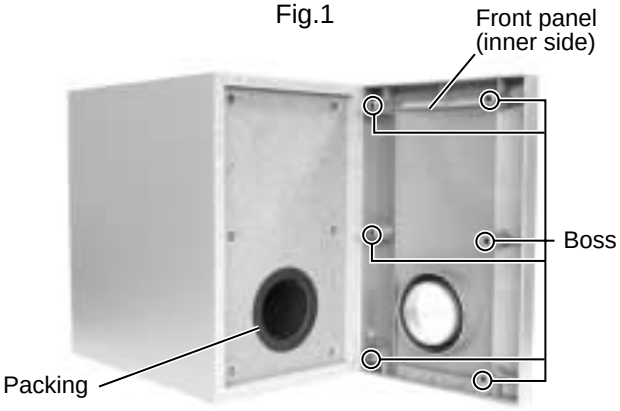


Fig.2

■ Removing the speaker unit

(See Fig.3 to 5)

1. Remove the four bosses and remove the net assembly.

   Notes: It will be good to use the tool with a flat tip, since it is hard to remove. Please take care not to damage the cabinet at this time.

2. Remove the eight screws **A** attaching the speaker unit to cabinet.

3. Disconnect the code from the two terminals of the speaker unit.

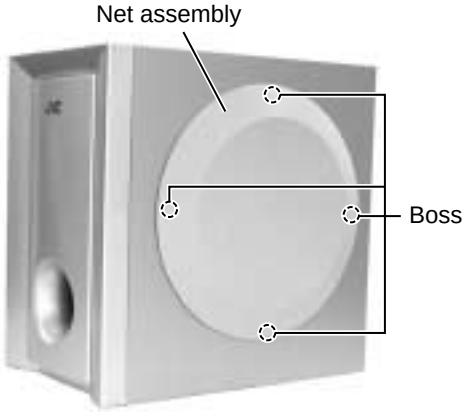
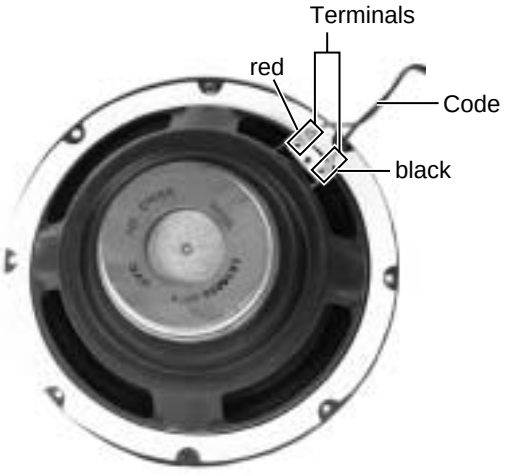


Fig.3



Speaker unit (reverse side)

Fig.5

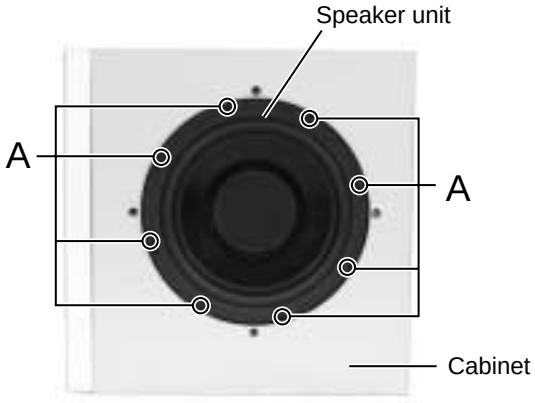
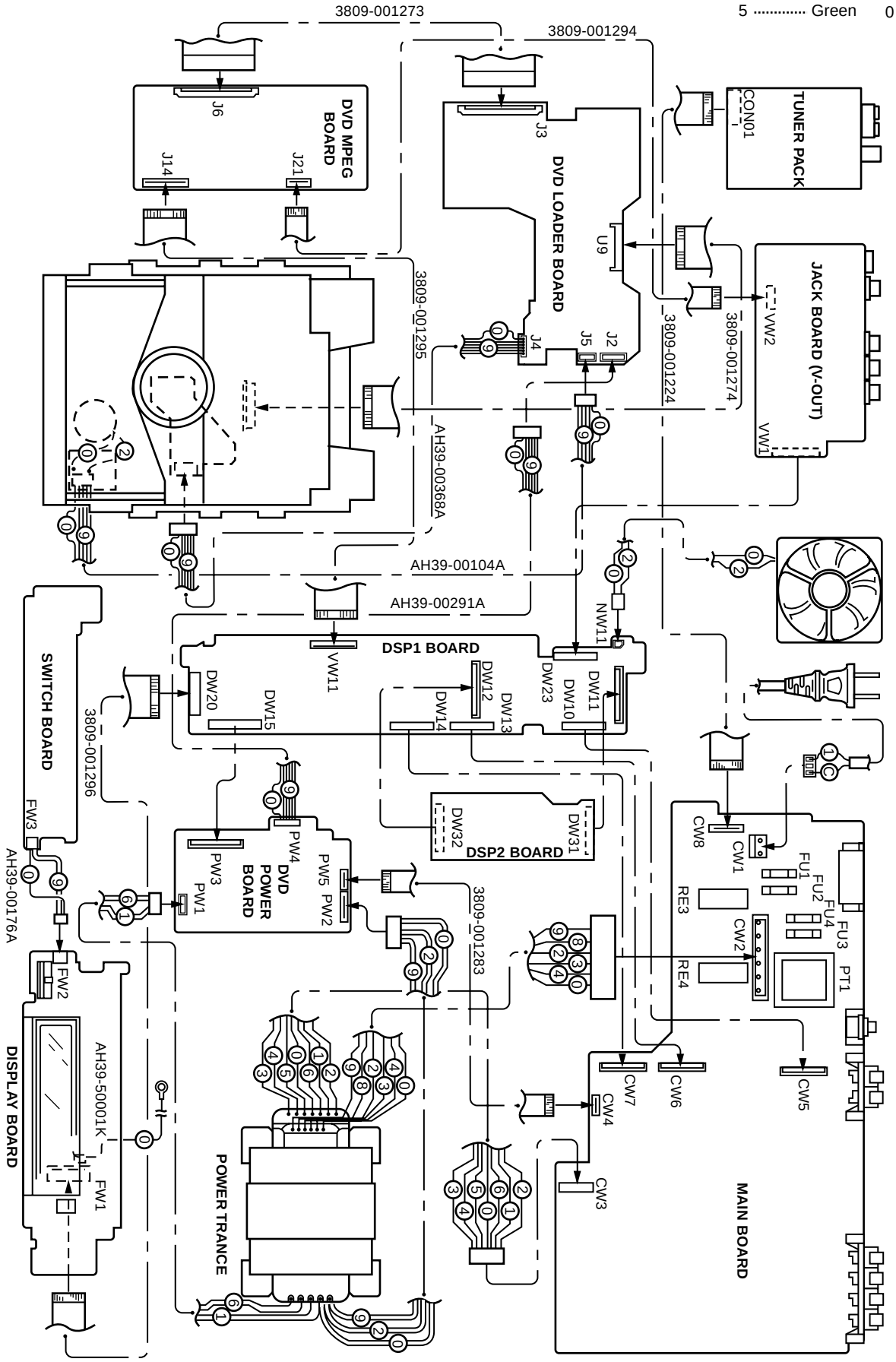


Fig.4

Wiring connection

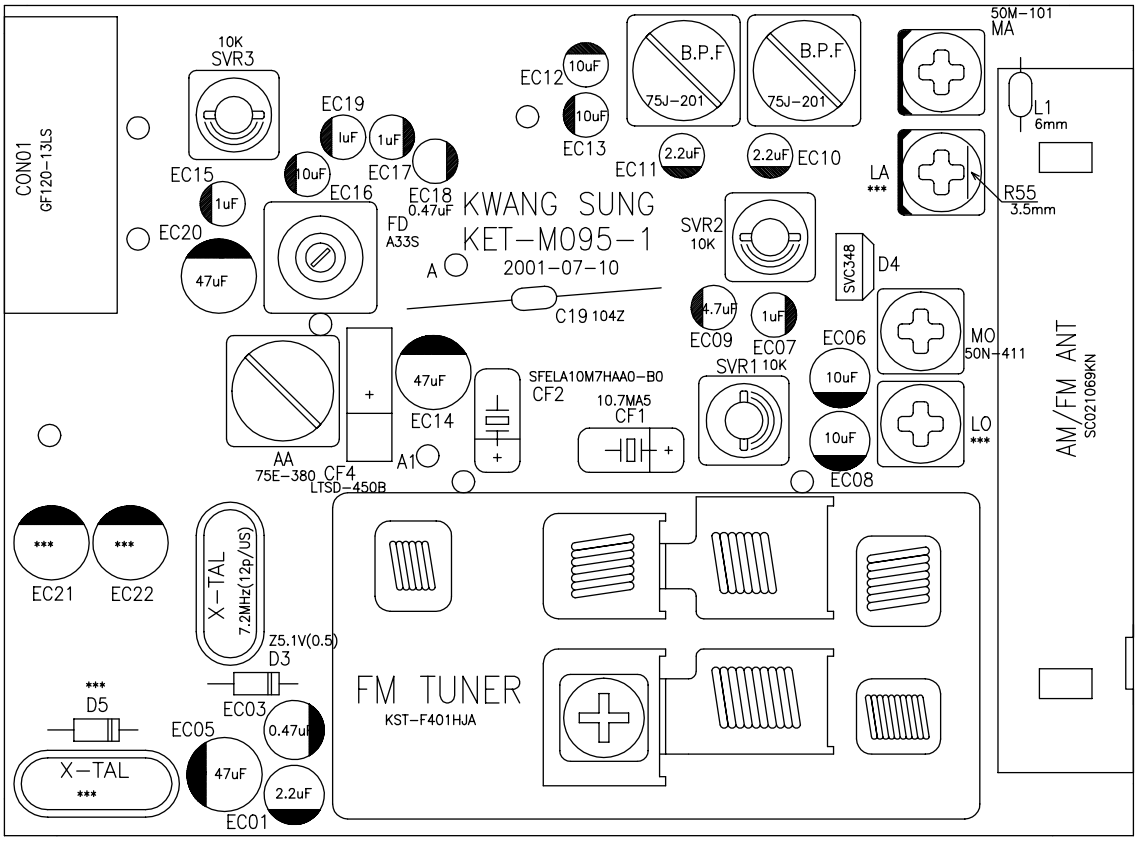
Color codes are shown below.

1	Brown	6	Blue
2	Red	7	Violet
3	Orange	8	Gray
4	Yellow	9	White
5	Green	0	Black



Adjustment method

1. Tuner



*Adjustment Location of Tuner PCB

ITEM	AM(MW) OSC Adjustment	AM(MW) RF Adjustment
Received FREQ.	A : 522~1629KHz (9k step) US/UB/ : 531~1602KHz (9k step) UW/UJ 530~1600KHz (10k step)	603 KHz
Adjustment point	MO	MA
Output	1~7.0V	Maximum Output(Fig1-1)

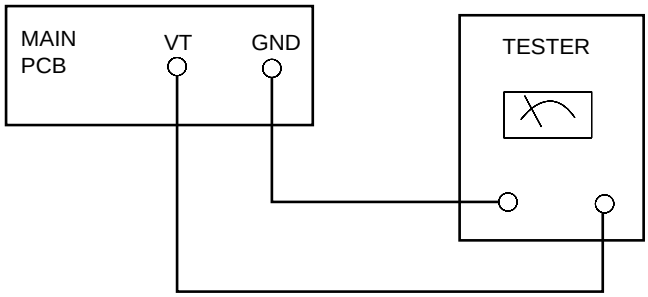


Fig 1-1 OSC Voltage

FM THD Adjustment	
SSG FREQ.	98 MHz
Adjustment point (FD)	FM DETECTOR COIL
Output	60 dB
Minimum Distortion (0.4% below) (Figure 1-2)	

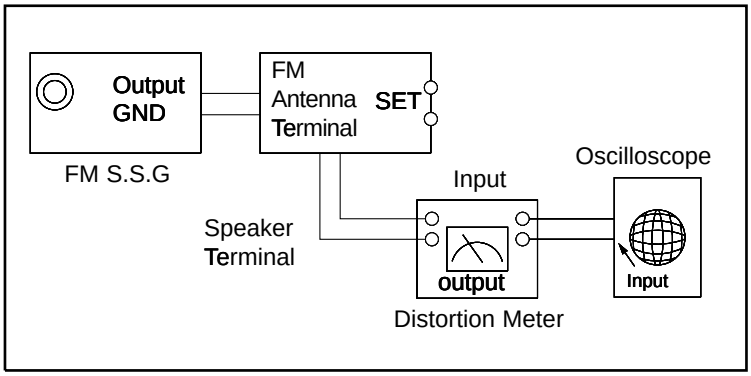


Figure1-2 IF CENTER and THD Adjustment

FM Search Level Adjustment	
SSG FREQ.	98 MHz
Adjustment point (SVR3)	BEACON SENSITIVITY SEMI-VR(20K)
Output	28 dB(dB)
Adjust SVR1 so that “TUNED” of FL T is lighted (Figure 1-3)	

*Adjust FM S.S.G level to 28dB

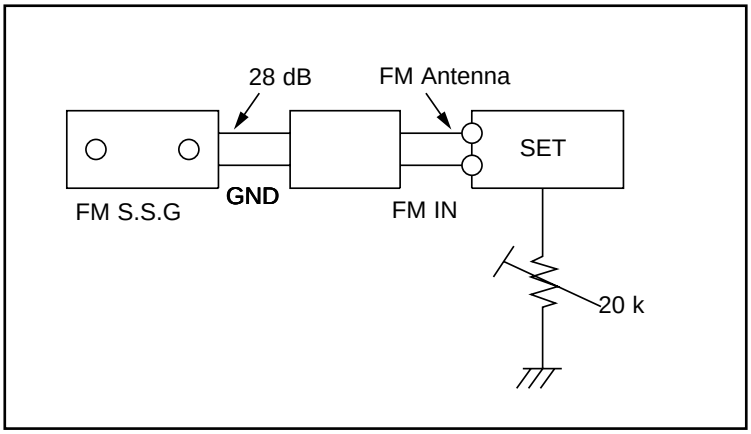


Figure1-3 FM Auto Search Level Adjustment

AM(MW) I.F Adjustment	
SSG FREQ.	450 kHz
Frequency	522 kHz
Adjustment point	AA
Maximum output (Figure 1-4)	

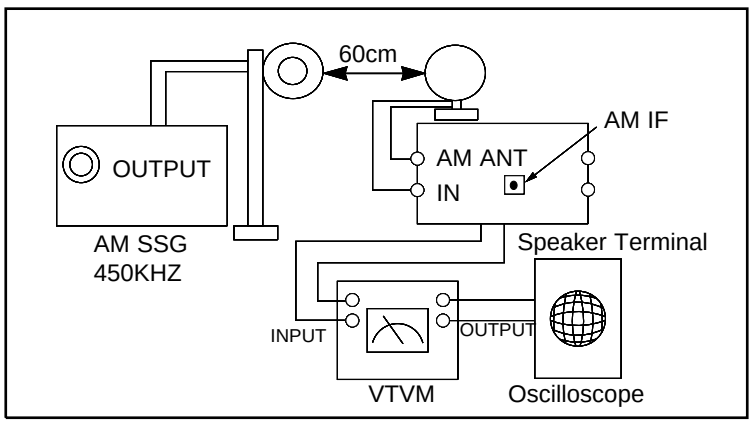


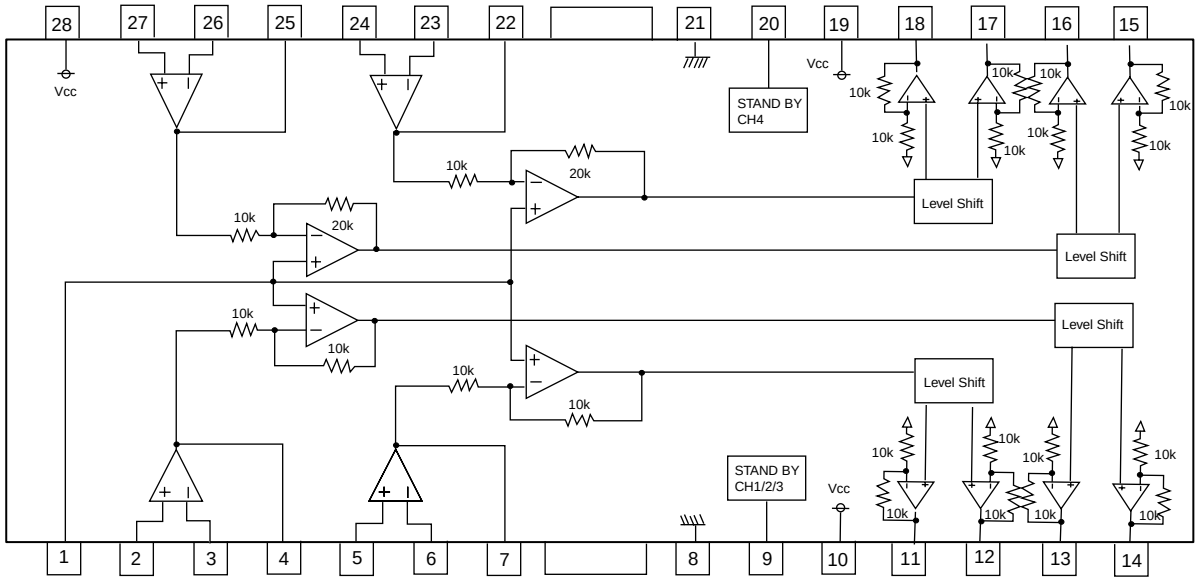
Figure1-4 AM I.F Adjustment

Notes: This set is a non-adjusted set fundamentally. It is adjusted when the tuner pack is exchanged.

Description of major ICs

■ BA5983FM (U6) : 4CH driver

1.Block diagram



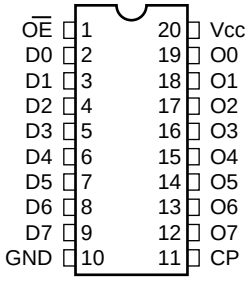
2.Pin function

Pin No.	Symbol	I/O	Function
1	BLAS IN	I	Input for Bias-amplifier
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP
4	OPOUT1	O	Output for CH1 OP-AMP
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP
7	OPOUT2	O	Output for CH2 OP-AMP
8	GND	-	Substrate ground
9	STBY1	I	Input for CH1/2/3 stand by control
10	PowVcc1	-	Vcc for CH1/2 power block
11	VO2(-)	O	Inverted output of CH2
12	VO2(+)	O	Non inverted output of CH2
13	VO1(-)	O	Inverted output of CH1
14	VO1(+)	O	Non inverted output of CH1

Pin No.	Symbol	I/O	Function
15	VO4(+)	O	Non inverted output of CH4
16	VO4(-)	O	Inverted output of CH4
17	VO3(+)	O	Non inverted output of CH3
18	VO3(-)	O	Inverted output of CH3
19	PowVcc2	-	Vcc for CH3/4 power block
20	STBY2	I	Input for Ch4 stand by control
21	GND	-	Substrate ground
22	OPOUT3	O	Output for CH3 OP-AMP
23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
25	OPOUT4	O	Output for CH4 OP-AMP
26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
28	PreVcc	-	Vcc for pre block

■ 74VHC574 (DIC16, DIC17) : Flip flop

1. Pin layout



2. Pin function

Symbol	Function
D0-D7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O0-O7	3-STATE Outputs

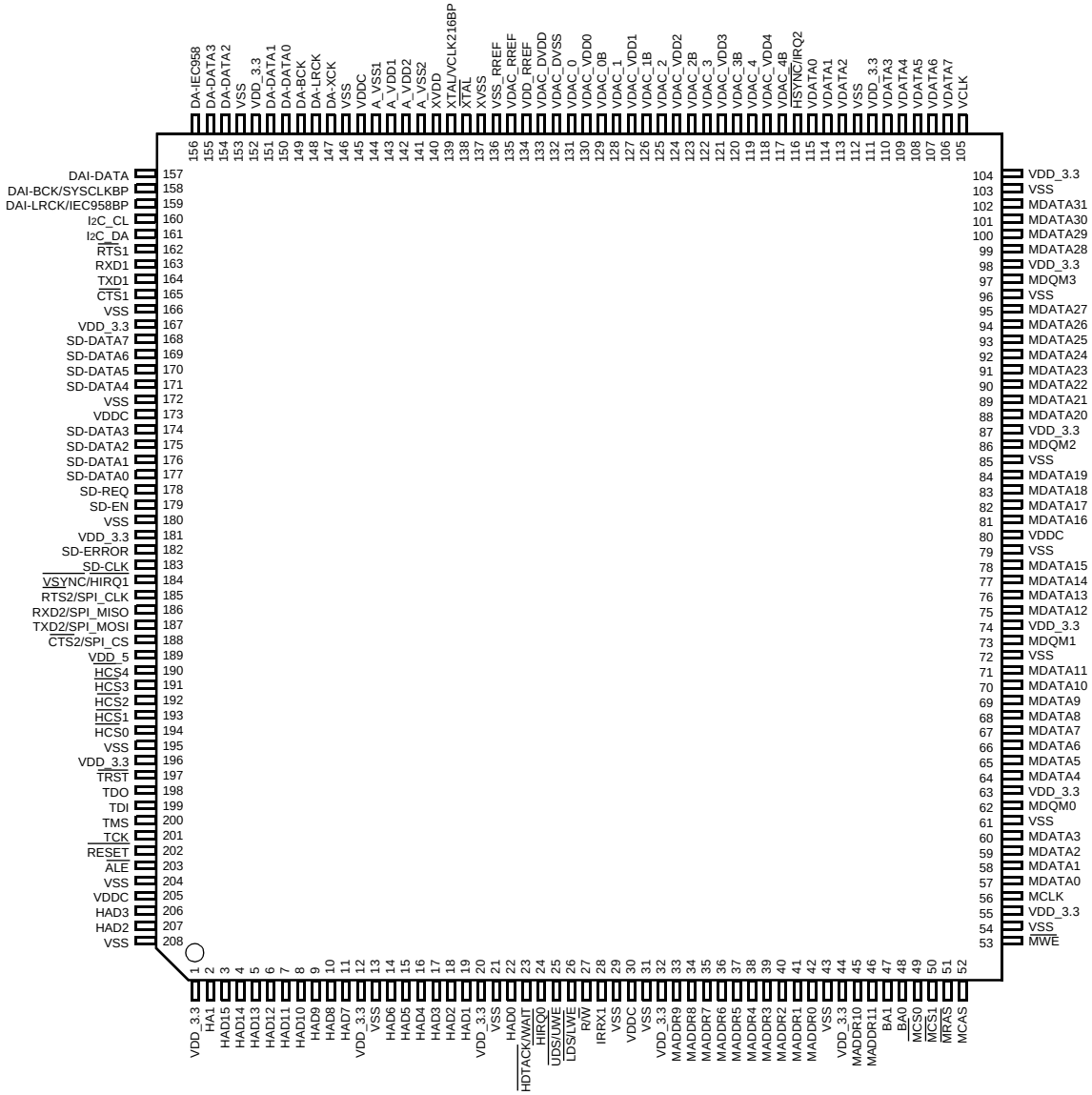
3. Truth table

Inputs			Outputs
Dn	CP	$\overline{OE}$	On
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H:HIGH Voltage Level
L:LOW Voltage Level
X:Immaterial
Z:High Impedance
⌐:HIGH to LOW transition

■ ZiVA-5 (U8) : DVD controller

1. Pin layout



2. Pin function (1/4)

	Name	Pin No.	Type [1]	Description
System Services	RESET	202	I	Active Low Reset. Assert for at least 5-milliseconds in the presence of clock to reset the entire chip.
	VCLK	105	I/O	Video clock that outputs 27 MHz.
	XOUT	138	O	Crystal output. When the internal DCXO is used, a 13.5 MHz crystal should be con-nected between this pin and the XIN pin.
	XIN/bypass clk_216	139	I	Crystal input. When the internal DCXO is used, a 13.5 MHz crystal should be con-nected between this pin and the XOUT pin. When an external oscillator or VCXO is used, its output should be connected to this pin. When configured for an external bypass clock, a 216 MHz clock should be connected to this pin. The frequency of an external VCXO can be either 27 or 13.5 MHz.

1. I - input, O - output, OD - open drain, PU - requires external pull-up resistor.

2. Pin function (2/4)

	Name	Pin No.	Type [1]	Description
Power and Ground	VNW	189	Power	5-V supply voltage for 5V-tolerant I/O signals.
	VDDP	12, 20, 111, 152, 167, 181, 196	Power	3.3-V supply voltage for I/O signals
	VDD25	32, 44, 55, 63, 74, 87, 98, 104	Power	3.3-V supply voltage for SDRAM I/O signals
	XVDD	140	Power	3.3V Crystal interface power
	VDD	30, 80, 145, 173, 205	Power	1.8-V supply voltage for core logic
	VDD_VDAC[4:0]	118, 121, 124, 127, 130	Power	Analog Video DAC Power
	VDAC_DVDD	133		3.3V Digital supply for 5 DACs
	A_VDD[2:1]	142, 143		3.3-V Analog PLL Power
	VDAC_REFVDD	134	Power	3.3V Analog Video Reference Voltage
	GNDP	13, 21, 112, 153, 166, 180, 195, 208	Ground	Ground for I/O signals
	GND	29, 79, 146, 172, 204	Ground	Ground for core logic
	GND25	31, 43, 54, 61, 72, 85, 96, 103	Ground	Ground for SDRAM I/O signals
	VDAC_DVSS	132	Ground	Digital VSS for DACs
	AVSS[2:1]	141, 144	Ground	Analog PLL Ground
	VDAC_REFVSS	136	Ground	Video Analog Ground
	XVSS	137	Ground	Crystal interface ground
Host Interface	$\overline{HCS}$[4:2]/GPIO[41:43]	190-192	O	Host chip select. Host asserts $\overline{HCS}$ to select the controller for a read or write operation. The falling edge of this signal triggers the read or write operation. General Purpose I/Os 41, 42, and 43, respectively.
	$\overline{HCS}$[1:0]	193, 192	I	Host chip select. Host asserts $\overline{HCS}$ to select the controller for a read or write operation. The falling edge of this signal triggers the read or write operation.
	HA[3:1]	206, 207, 2	I/O	Host (muxed address) address bus. 3-bit address bus selects one of eight host inter-face registers. These signals are not muxed in ATAPI master mode.
	HA[15:0]	3-11, 14-19, 22	I/O	HA[15:0] is the 16-bit (muxed address and data) bi-directional host data bus through which the host writes data to the decoder Code FIFO. MSB of the 32-bit word is writ-ten first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HA[7:0]. These signals are not muxed for ATAPI master mode.
	$\overline{HDTACK}$/WAIT	23	I/OD	Host Data Transfer Acknowledge.
	$\overline{HIRQ0}$	24	I/O	Host interrupt. Open drain signal, must be pulled-up via 4.7kΩto 3.3 volts. Driven high for 10 ns before tristate.
	$\overline{HUDS}$/UWE	25	I/O	Host Upper Data Strobe. Host high byte data, HA[15:8], is valid when this pin is active.
	$\overline{HLDS}$/$\overline{LWE}$	26	I/O	Host Lower Data Strobe. Host low byte data, HA[7:0], is valid when this pin is active.
	HREAD	27	I/O	Read/write strobe
	$\overline{ALE}$	203	I/O	Address latch enable
SDRAM Interface	$\overline{MCS}$[1:0]	50, 49	O	Memory chip select.
	$\overline{MCAS}$	52	O	Active LOW SDRAM Column Address Strobe.
	$\overline{MRAS}$	51	O	Active LOW SDRAM Row Address Strobe.
	MDQM[3:0]	97, 86, 73, 62	O	These pins are the bytes masks corresponding to MD[7:0], [15:8], [23:16] and [31:24]. They allow for byte reads/writes to SDRAM.
	MA[11:0]	46, 45, 33-42	O	SDRAM Address
	MD[31:0]	102-99, 95-88, 84-81, 78-75, 71-64, 60-57	I/O	SDRAM Data
	$\overline{MWE}$	53	O	SDRAM Write Enable. Specifies transaction to SDRAM: read (=1) or write (=0)
	MCLK	56	O	SDRAM Clock
	BA[1:0]	47, 48	O	SDRAM bank select
Digital Video Input/Output	$\overline{HSYNC}$/$\overline{HIRQ2}$/ GPIO1[9]	116	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of HSYNC. Host Interrupt Request 2 General Purpose I/O 9
	VCLK	105	I/O	Video clock. Clocks out data on input. VDATA[7:0]. Clock is typically 27 MHz.
	VDATA[7:0]/GPIO[1:7]	106-110, 113-115	I/O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At powerup, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA. General Purpose I/Os [1:7]
	$\overline{VSYNC}$/$\overline{HIRQ1}$/ GPIO36	184	I/O	Vertical sync. Bi-directional, the decoder outputs the top border of a new field on the first $\overline{HSYNC}$ after the falling edge of $\overline{VSYNC}$. $\overline{VSYNC}$ can accept vertical synchroni-zation or top/bottom field notification from an external source. ($\overline{VSYNC}$ HIGH = bot-tom field. $\overline{VSYNC}$ LOW = Top field) Active Low Host Interrupt Pin General Purpose I/O 36

1. I - input, O - output, OD - open drain, PU - requires external pull-up resistor.

2. Pin function (3/4)

	Name	Pin No.	Type [1]	Description
Parallel DVD/CD or Serial CD Interface	SDDATA[7]/VDATA2[7] /HDMARQ/GPIO24	168	I	Compressed data from DVD DSP. Bit 7. In parallel mode, bit 7 is the first (earliest in time) bit in the bitstream, while bit 0 is the last bit. Video Data Bus 2, Bit 7 Host DMA Request General Purpose I/O 24
	SDDATA6/VDATA2[6] /HXCVR_EN/GPIO25	169		Compressed data from DVD DSP. Bit 6. Video Data Bus 2, Bit 6 ATAPI Transceiver Enable General Purpose I/O 25
	SDDATA5/VDATA2[5] HDMACK/GPIO26	170		Compressed data from DVD DSP. Bit 5. Video Data Bus 2, Bit 5 Host DMA Acknowledge General Purpose I/O 26
	SDDATA4/VDATA2[4]/ GPIO27	171		Compressed data from DVD DSP. Bit 4. Video Data Bus 2, Bit 4 General Purpose I/O 27
	SDDATA3/ VDATA2[3]/GPIO28	174		Compressed data from DVD DSP. Bit 3. Video Data Bus 2, Bit 3 General Purpose I/O 28
	SDDATA2/ VDATA2[2]/GPIO29	175		Compressed data from DVD DSP. Bit 2. Video Data Bus 2, Bit 2 General Purpose I/O 29
	SDDATA1/ VDATA2[1]/GPIO30	176		Compressed data from DVD DSP. Bit 1. Video Data Bus 2, Bit 1 General Purpose I/O 30
	SDDATA0/ VDATA2[0]/GPIO31	177		In serial mode, bit 0 should be used as the input, with the unused bits either used as GPIOs or tied to ground. Video Data Bus 2, Bit 0 General Purpose I/O 31
	SDCLK	183	I	Data clock. The maximum frequency is 25 MHz for parallel mode, and ???? MHz for serial mode. The polarity of this signal is programmable.
	SDERROR	182	I	Error in input data. This signal carries the error bit associated with the channel data type (if set, the byte is corrupted).
	SDEN/GPIO33	179	I	Data enable. Assertion indicates that data on SDDATA[7:0] is valid. The polarity of this signal is programmable. General Purpose I/O [33]
	SDREQ/GPIO32	178	O	Bitstream request. controller asserts SDREQ to indicate that the bitstream input buffer has available space. General Purpose I/O 32
Analog Video Output	VDAC_[4B:0B]	117, 120, 123, 126, 129	Analog O	Video DAC Bias Bits[4:0]
	VDAC_4	119	Analog O	DAC video output format: R, V, C, or CVBS. Macrovision encoded.
	VDAC_3V	122	Analog O	DAC video output format: B, U, C, or CVBS. Macrovision encoded.
	DAC_2	125	Analog O	DAC video output format: G or Y. Macrovision encoded.
	VDAC_1	128	Analog O	DAC video output format: C. Macrovision encoded.
	VDAC_0	131	Analog O	DAC video output format: CVBS or Y. Macrovision encoded.
	VDAC_REF	135	Analog I	Video DACs Reference Resistor. Connecting to pin 136 through a 1.18K+/- 1% resis-tor is required.
	VCLK	105	I/O	System clock that drives internal PLLs. ZiVA-5 27-MHz TTL oscillator. (See descrip-tion of VCLK for Digital Video Output.) Also optional video clock for internal PLLs or external encoder.
Audio Interface	ADATA[3:0]/GPIO[4:1]	155, 154, 151, 150	O	PCM Data Out. Eight channels. Serial audio samples relative to BCK and LRCK. General Purpose I/Os [4:1]
	BCK	149	O	PCM Bit Clock. BCK can be either 48 or 32 times the sampling frequency
	LRCK	148	O	PCM Left Clock. Identifies the channel for each sample. The polarity is programma-ble.
	XCK	147	I/O	Audio External Frequency clock input or output. BCK and LRCK are derived from this clock.
	IEC958/GPIO14	156	O	PCM data out (IEC-958 format) or compressed data out (IEC-1937 format). General Purpose I/O [14]
Digital Mic In	DAI_DATA/GPIO15	157	I	PCM data input. General Purpose I/O [15]
	DAI_BCK/ BYPASS_SYSCLK/ GPIO16	158	I	PCM input bit clock. BYPASS_SYSCLK: Alternate function TBS. General Purpose I/O [16]
	DAI_LRCK/ IEC958BP/GPIO17	159	I	PCM left/right clock. IEC958 input bypass General Purpose I/O [17]

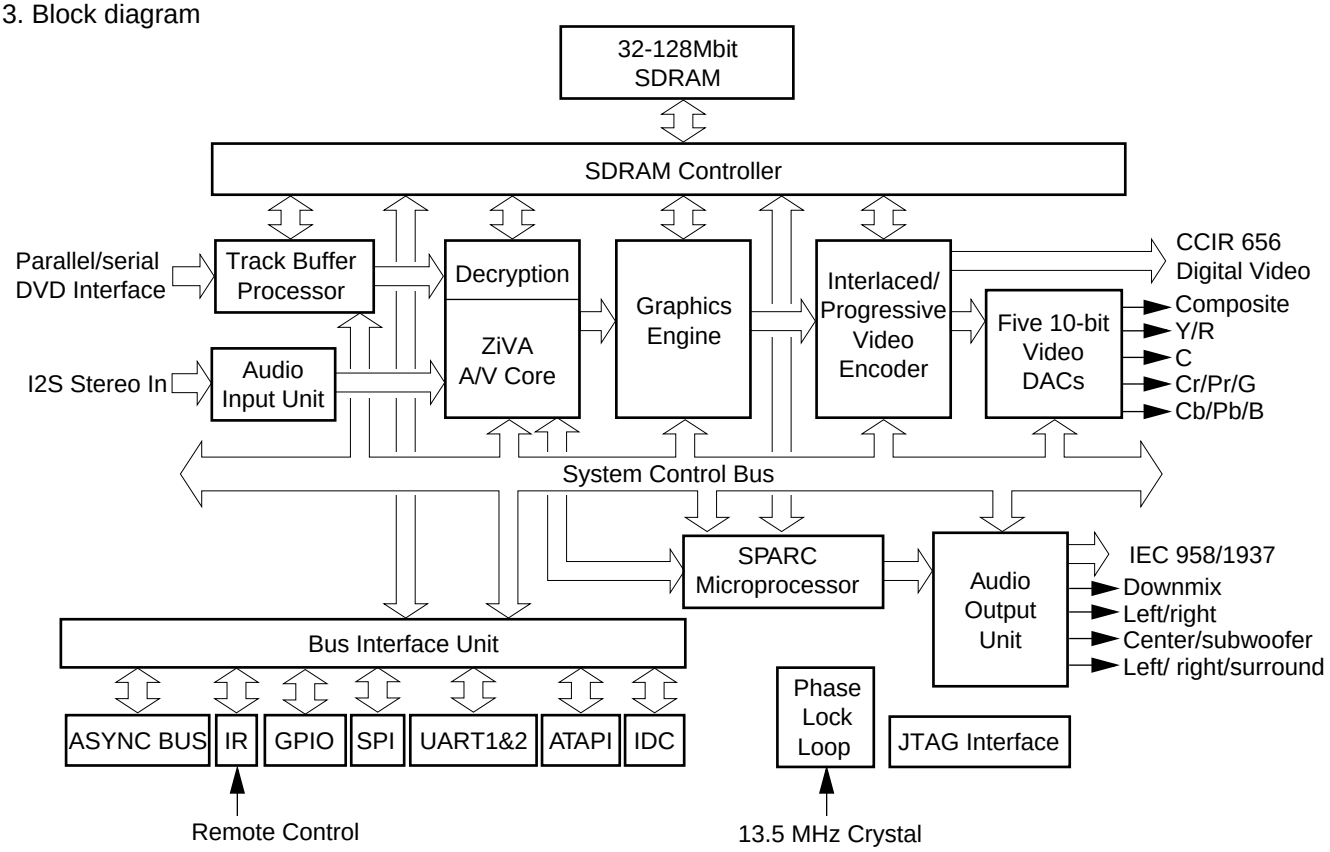
1. I - input, O - output, OD - open drain, PU - requires external pull-up resistor.

2. Pin function (4/4)

	Name	Pin No.	Type [1]	Description
IR	IRRX1/GPIO0	28	I	IR Remote Receive. This input connects to an integrated (photo diode, band pass, demodulator) IR receiver. General Purpose I/O 0
IDC	IDC_CL/GPIO18	160	I/O	Serial clock signal for IDC data transfer. It should be pulled up to the positive supply voltage, depending on the device) using an external pull-up resistor. General Purpose I/O [18]
	IDC_DA/GPIO19	161		Serial data signal for IDC data transfer. It should be pulled up to the supply voltage using an external pull-up resistor. General Purpose I/O [19]
UART1	$\overline{RTS1}$/GPIO20	162	O	Ready to send, UART1 General Purpose I/O [20]
	RXD1/GPIO21	163	I	Receive data, UART1 General Purpose I/O [21]
	TXD1/GPIO22	164	O	Transmit data, UART1 General Purpose I/O [22]
	$\overline{CTS1}$/GPIO23	165	I	Clear to send, UART1 General Purpose I/O [23]
UART2	$\overline{RTS2}$/SPI_CLK/ GPIO37	185	O	Ready to send, UART2 Serial Peripheral Interface Clock General Purpose I/O [37]
	RXD2/SPI_MISO/ GPIO38	186	I	Receive data, UART2 Serial Peripheral Interface - Master Input/Slave Output General Purpose I/O [38]
	TXD2/SPI_MOSI/ GPIO39	187	O	Transmit data, UART2 Serial Peripheral Interface - Master Output/Slave Input General Purpose I/O [39]
	$\overline{CTS2}$/SPI_CS/ GPIO40	188	I	Clear to send, UART2 Serial Peripheral Interface ???? General Purpose I/O [40]
JTAG	$\overline{TRST}$	197	I	Test reset. BST reset - resets the TAP controller. This signal must be pulled low.
	TDO	198	O	Test data Out. BST serial data output.
	TDI/GPI0	199	I	Test data In. BST serial data chain input. General Purpose Input pin 0.
	TMS/GPI1	200	I	Test mode select. Controls state of test access port (TAP) controller. General Purpose Input pin 1.
	TCK	201	I	Test clock. Boundary scan test (BST) serial data clock.

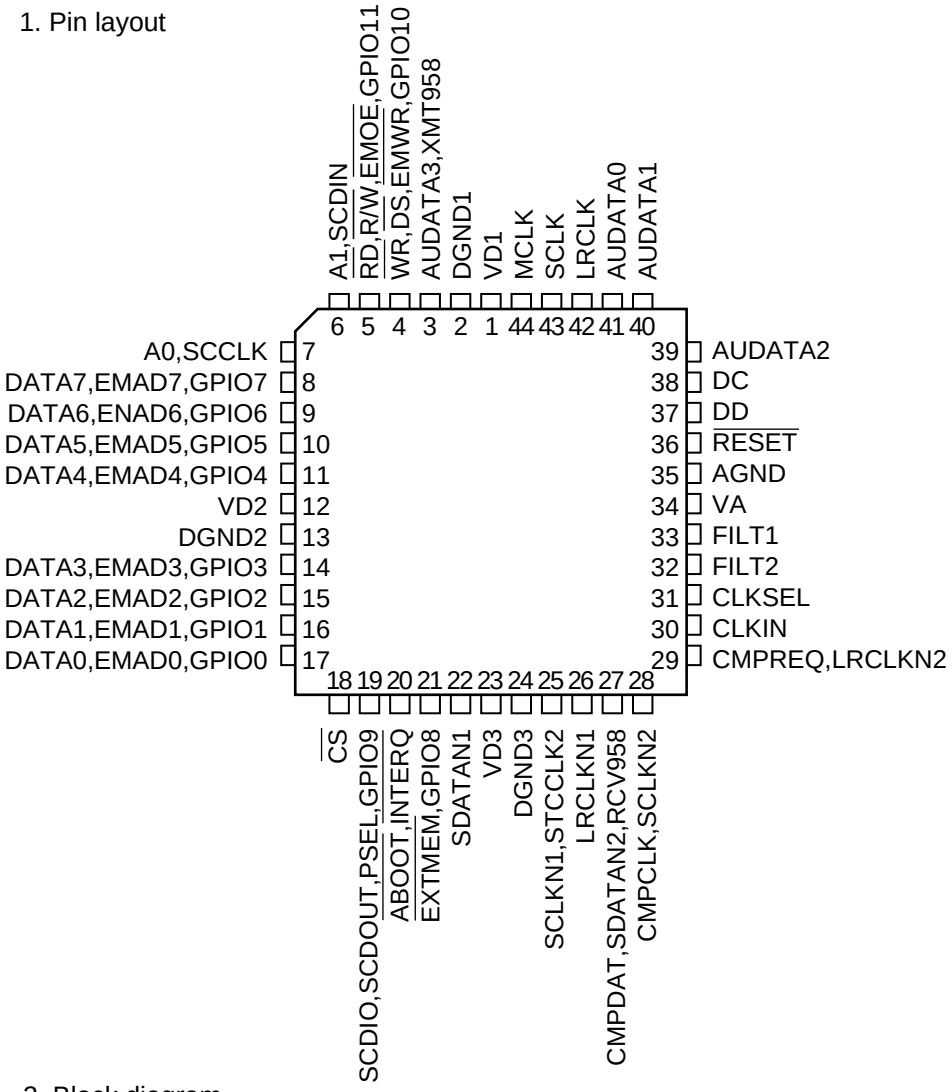
1. I - input, O - output, OD - open drain, PU - requires external pull-up resistor.

3. Block diagram

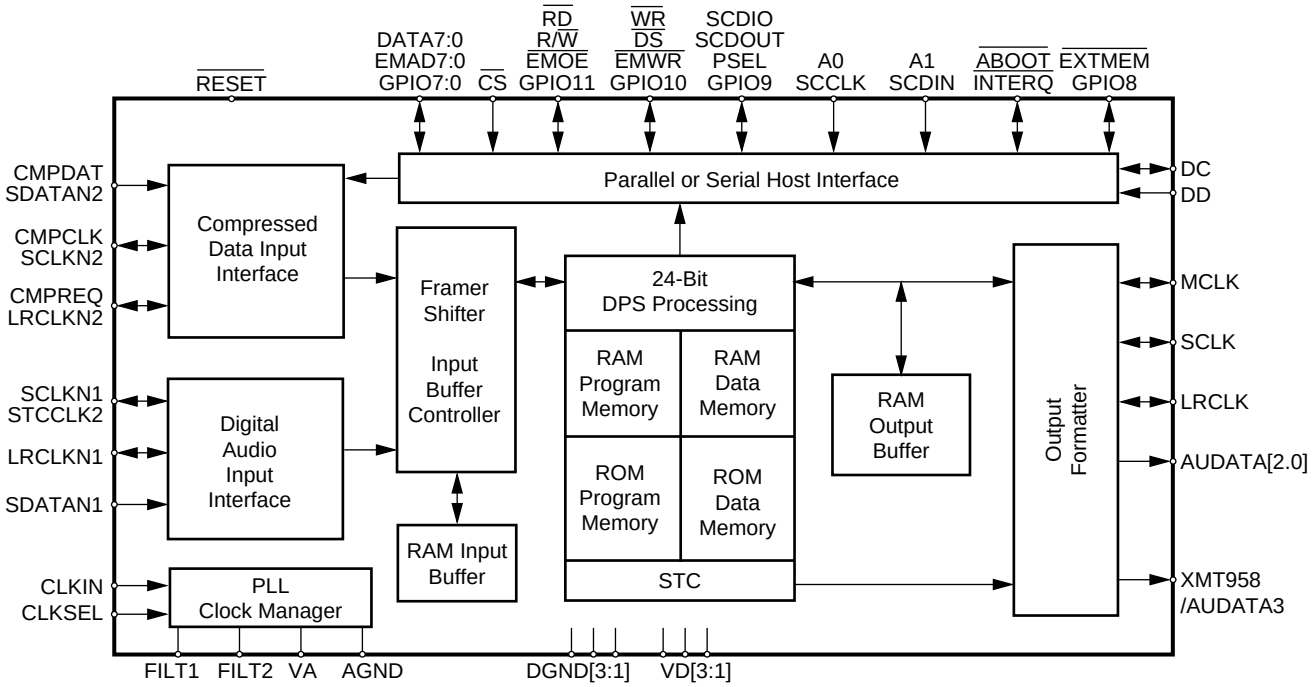


■ CS493292 (DIC11) : Audio decoder

1. Pin layout



2. Block diagram

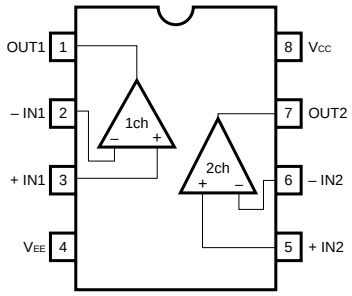


3. Pin function

Pin No.	Symbol	Function
1,12,23	VD1,VD2,VD3	Digital Positive Supply
2,13,24	DGND1,DGND2,DGND3	Digital Supply Ground
3	AUDATA3,XMT958	SPDIF Transmitter Output, Digital Audio Output 3
4	WR,DS,EMWR,GPIO10	Host write strobe or Host data strobe or External Memory write enable or General purpose input& output Number 10
5	RD,R/W,EMOE,GPIO11	Host Parallel Output Enable or Host Parallel R/W or External Memory Output Enable or General Purpose Input & Output Number11
6	A1,SCDIN	Host Address Bit One or SPI Serial Control Data Input
7	A0,SCCLK	Host Parallel Address Bit Zero or Serial Control Port Clock
8	DATA7,EMAD7,GPIO7	Data Bus
9	DATA6,ENAD6,GPIO6	Data Bus
10	DATA5,EMAD5,GPIO5	Data Bus
11	DATA4,EMAD4,GPIO4	Data Bus
14	DATA3,EMAD3,GPIO3	Data Bus
15	DATA2,EMAD2,GPIO2	Data Bus
16	DATA1,EMAD1,GPIO1	Data Bus
17	DATA0,EMAD0,GPIO0	Data Bus
18	CS	Host Parallel Chip Select, Host Serial SPI Chip Select
19	SCDIO,SCDOUT,PSEL,GPIO9	Serial Control Port Data Input and Output, Parallel Port Type Select
20	ABOOT,INTERQ	Control Port Interrupt Request, Automatic Boot Enable
21	EXTMEM,GPIO8	External Memory Chip Select or General Purpose Input & Output Number 8
22	SDATAN1	PCM Audio Data Input Number One
25	SCLKN1,STCCLK2	PCM Audio Input Bit Clock
26	LRCLKN1	PCM Audio Input Sample Rata Clock
27	CMPDAT,SDATAN2	PCM Audio Data Input Number Tow
28	CMPCLK,SCLKN2	PCM Audio Input bit Clock
29	CMPREQ,LRCLKM2	PCM Audio Input Sample Rate Clock
30	CLKIN	Master Clock Input
31	CLKSEL	DSP Clock Select
32	FILT1	Phase Locked Loop Filter
33	TILT2	Phase-Locked Loop Filter
34	VA	Analog Positive Supply
35	AGND	Analog Supply Ground
36	RESET	Master Reset Input
37	DC	Reserved
38	DD	Reserved
39	AUDATA2	Digital Audio Output 2
40	AUDATA1	Digital Audio Output 1
41	AUDATA0	Digital Audio Output 0
42	LRCLK	Audio Output Sample Rate Clock
43	SCLK	Audio Output Bit Clock
44	MCLK	Audio Master Clock

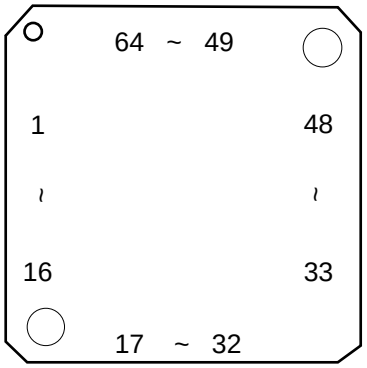
■ BA4560 (IC2, IC5, IC6, IC7, CIC11, CIC13, FIC2, FIC4, FIC5, FIC6, FIC11, RIC11, RIC13) : Dual op amp.

1.Pin layout



■ SP3721A (U7) : DVD driver

1.Pin layout



2.Pin function (1/2)

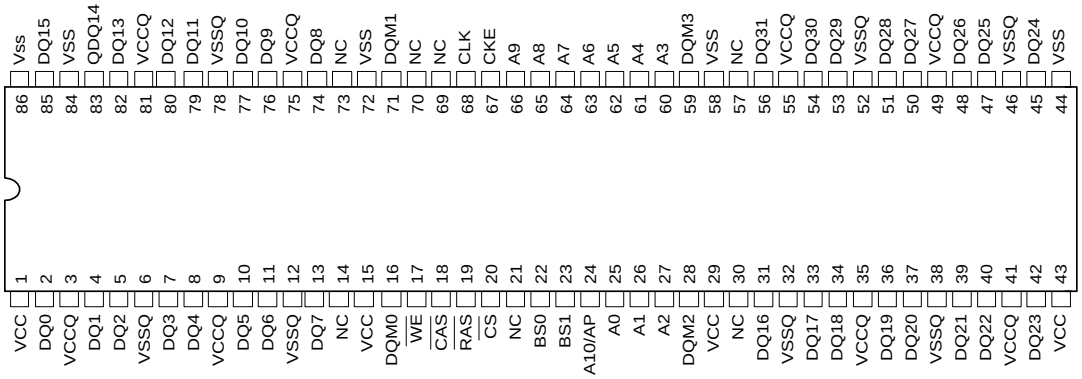
Pin No.	Symbol	I/O	Function
1	DVDRFP	I	RF Signal Inputs. Differential RF signal attenuator input pins.
2	DVDRFN		
3,4	PD1,PD2	I	CD Photo detector Interface Inputs. Inputs from the CD photo detector error outputs.
5~6	A2,B2	I	Photo Detector Interface Inputs. AC coupled inputs for the DPD from
7~ 8	C2,D2		the main beam Photo detector matrix outputs.
9	CP	I/O	Differential Phase tracking LPF pin. An external capacitance is connected between this pin and the CN pin.
10	CN	I/O	Differential Phase tracking LPF pin. An external capacitance is connected between this pin and the CP pin.
11~14	A,B,C,D	I	Photo Detector Interface Inputs. Inputs from the main beam Photo detector matrix outputs.
15~16	E,F	I	CD tracking Error Inputs. Inputs from the CD photo detector error outputs.
17	CDTE	-	CD Tracking. E-F Opamp output for feedback.
18	VCI2	-	Reference Voltage input. DC bias voltage input for the servo input reference.
19	NC	-	No Connect.
20	VNB	-	Ground. Ground pin for the servo block.
21	DVDPD	I	APC Input. DVD APC input pin from the monitor photo diode.
22	DVDLD	O	APC output. DVD APC output pin to control the laser power.
23	CDPD	I	APC Input. DVD APC input pin from the monitor photo diode.
24	CDLD	O	APC output. DVD APC output pin to control the laser power.
25	LDON#	I	APC output. on/off. APC output control pin. A low level activates the LD output. (open high)
26	VC	-	Reference Voltage output. This pin provides the internal DC bias reference voltage (+2.5+ fix). Output impedance is less than 50 ohms.
27	VCI	-	Reference Voltage input. DC bias voltage input for the servo input reference.
28	VPB	-	Power. Power supply pin for the servo block.
29	MIRR	O	Mirror Detect Output. Mirror Detect comparator output. Pseudo CMOS output.
30	MP	-	MIRR signal Peak hold pin. An external capacitance is connected to between this pin and VPB.
31	MB	-	MIRR signal Bottom hold pin. An external capacitance is connected to between this pin and VPB.
32	FDCHG#	I	Low Impedance Enable. A TTL compatible input pin that activates the FDCHG switches. A low level activates the switches and the falling edge of the internal FDCHG triggers the fast decay for the NIRR bottom hold circuit. (open high)
33	MLPF	-	MIRR signal LPF pin. An external capacitance is connected between this pin and VPB.

2.Pin function (2/2)

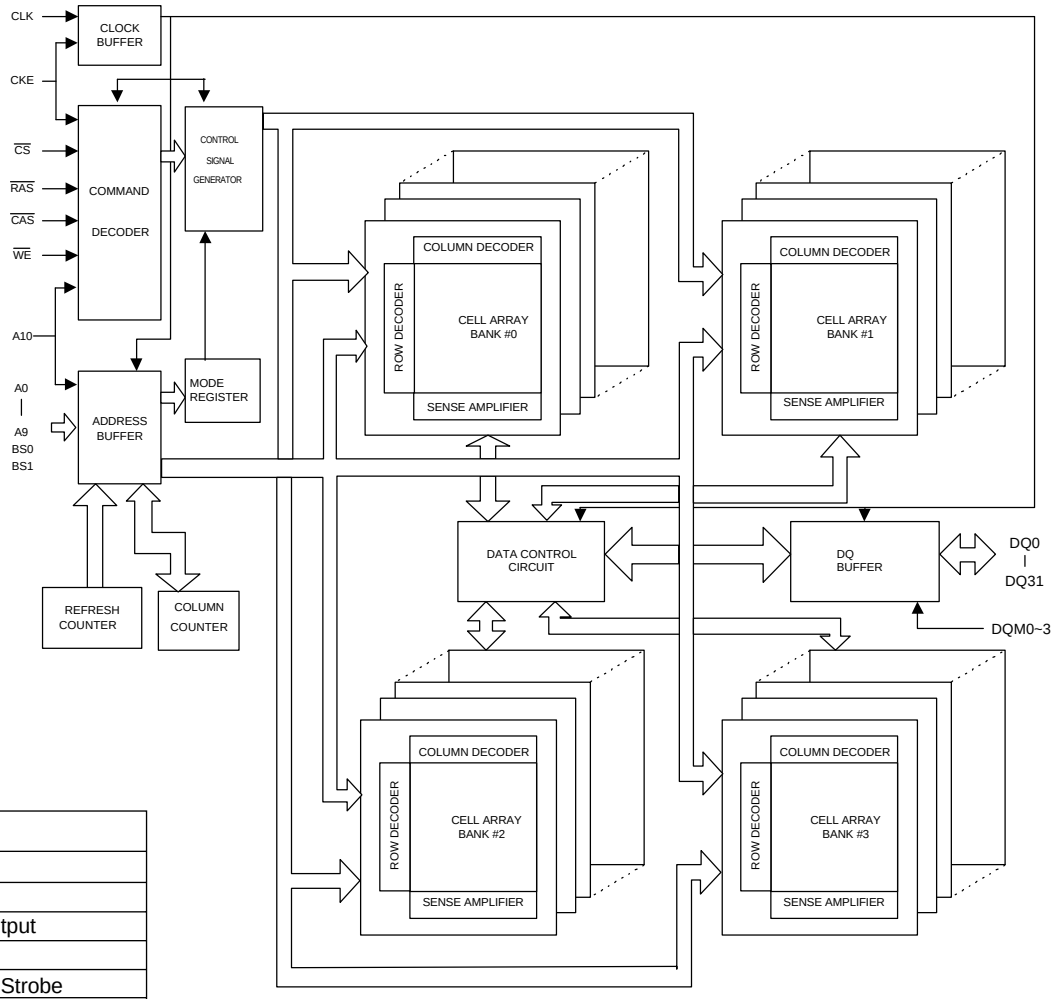
Pin No.	Symbol	I/O	Function
34	MEVO	O	SIGO Bottom Envelope Output. Bottom envelope for Mirror detection.
35	MIN	I	RF signal Input for Mirror. AC coupled inputs for the mirror detection circuit from the pull-in signal output. (PI)
36	PI	O	Pull-in Signal Output. The summing signal output of A,B,C,D or PD1, PD2 for mirror detection. Reference to VCI.
37	DFT	O	Defect Output. Pseudo CMOS output. When a defect is detected, the DFT output goes high. Also the servo AGC output can be monitored at this pin, When CAR bits 7-4 are '0011'.
38	TPH	-	PI Top Hold pin. An external capacitance is connected between this pin and VPB.
39	MEV	-	SIGO Bottom Envelope pin. An external capacitance is connected between this pin and VPB.
40	MEI	I	Mirror Envelope Input. The SIGO envelope input pin.
41	TE	O	Tracking Error Signal Output. Tracking error output reference to VCI.
42	FE	O	Focusing Error Signal Output. Focus error output reference to VCI.
43	CE	O	Center Error Signal Output. Center error out put reference to VCI.
44	LCN	-	Center Error LPF pin. An external capacitance is connected between this pin and the LCP pin.
45	LCP	-	Center Error LPF pin. An external capacitance is connected between this pin and the LCN pin.
46	SCLK	I	Serial Clock. Serial Clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA. (Not to be left open).
47	SDATA	I/O	Serial Data. Serial data bi-directional CMOS pin. NRZ programming data for the internal registers is applied to this input. (Not to be left open)
48	SDEN	I	Serial Data Enable. Serial enable CMOS input. A high level input enables the serial port. (Not to be left open)
49	HOLD1	I	Hold Control. ATTL compatible control pin which, when pulled high, disables the RF AFC charge pump and holds the RE AGC amplifier gain at its present value. (open high)
50	VNA	-	Ground. Ground pin for the RF block and serial port.
51	FNN	O	Differential Normal Output. Filter normal outputs.
52	FNP	O	Differential Normal Output. Filter normal outputs.
53	DIP	I	Analog inputs for RF Single Buffer. Differential analog inputs to the RF single-ended output buffer and full wave rectifier.
54	DIN	I	Analog inputs for RF Single Buffer. Differential analog inputs to the RF single-ended output buffer and full wave rectifier.
55	RX	-	Reference Resistor Input. An external 8.2 kohm, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.
56	BYP	I/O	The RF AGC integration capacitor CBYP, is connected between BYP and VPA.
57	SIGO	O	Single Ended Normal Output. SIngle-ended RF output.
58	VPA	-	Power. Power supply pin for the RF block and serial port.
59	AIP	I	AGC Amplifier Inputs. Differential AGC amplifier input pins.
60	AIN	I	AGC Amplifier Inputs. Differential AGC amplifier input pins.
61	ATON	O	Differential Attenuator Output. Attenuator outputs.
62	ATOP	O	Differential Attenuator Output. Attenuator outputs.
63	CDRF	I	RF Signal Input. Single-ended RF signal attenuator input pin.
64	CDRFDC	O	CD RF Signal Output. Single ended CD RF summing output.

■ W986432DH (U5) : SDRAM

1. Pin layout



2. Block diagram

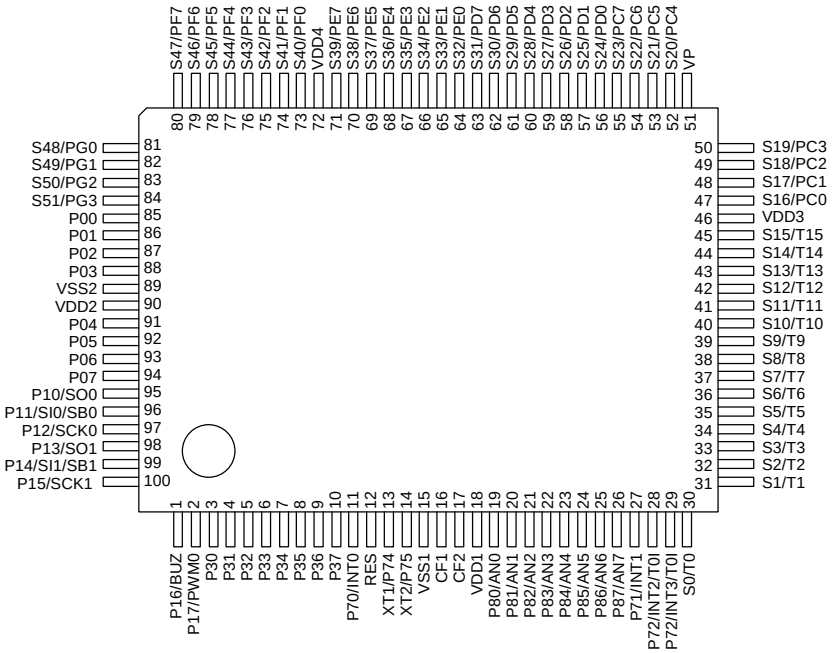


3. Pin function

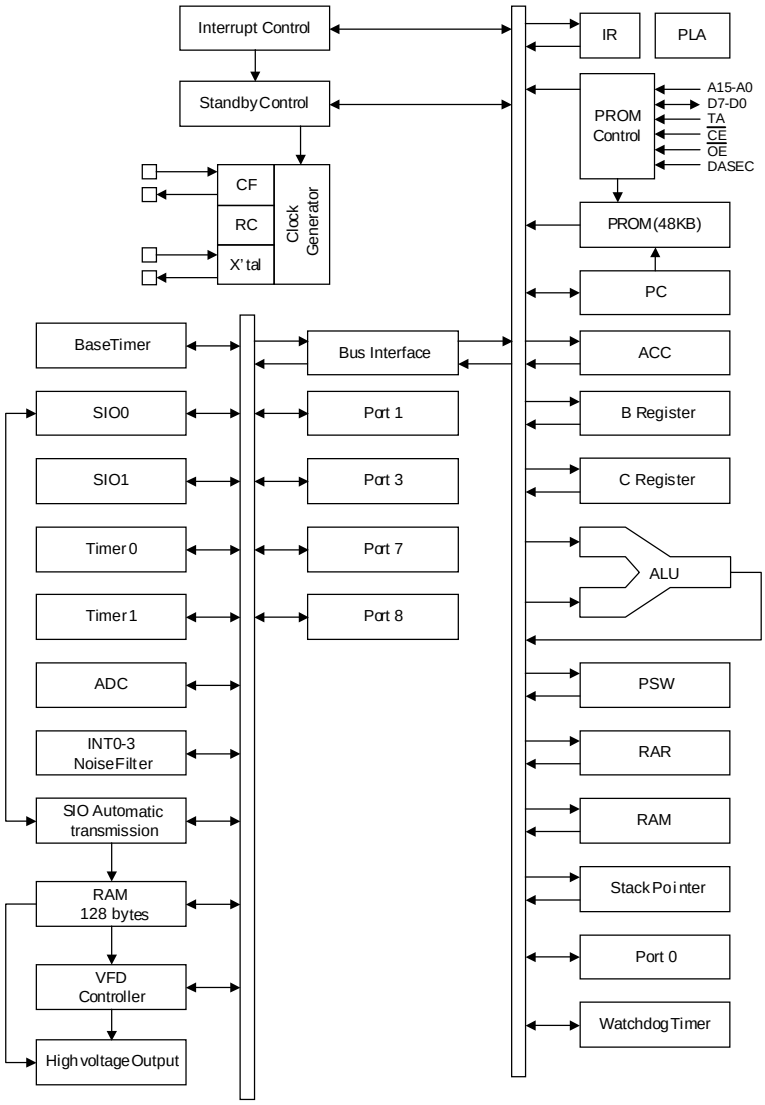
Symbol	Function
A0-A10	Address
BS0, BS1	Bank Select
DQ0-DQ31	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0-DQM3	Input/output mask
CLK	Clock Inputs
CKE	Clock Enable
VCC	Power(+3.3V)
VSS	Ground
VCCQ	Power(+3.3V) for I/O buffer
VSSQ	Ground for I/O buffer
NC	No Connection

■ LC86P6548 (UIC1) : Microcontroller

1.Pin layout

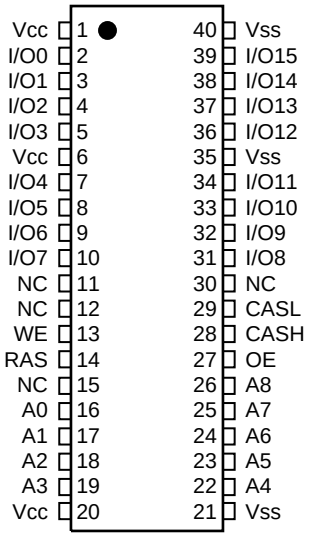


2.Block diagram



■ M11B416256A (U1) : DRAM

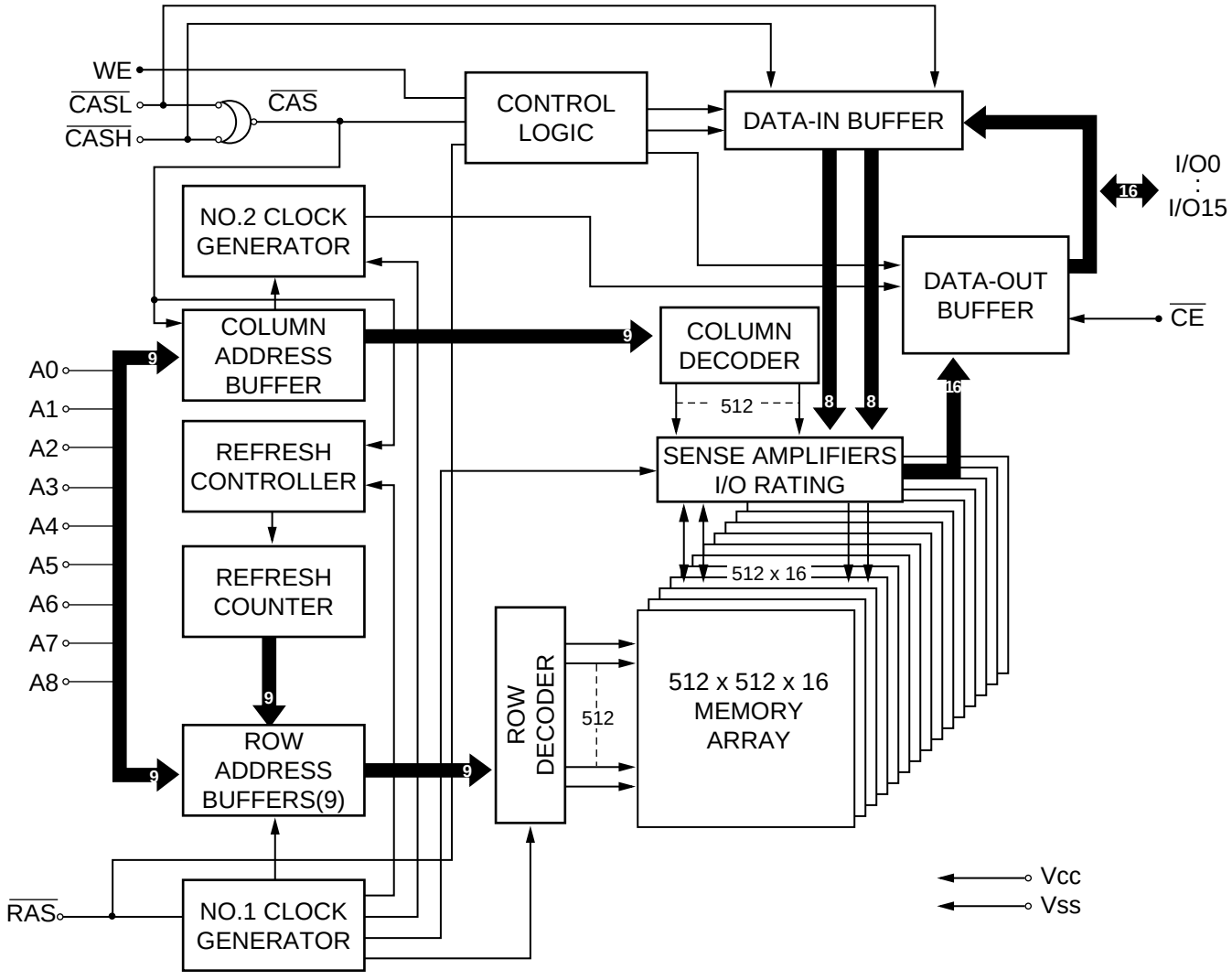
1. Pin layout



2. Pin function

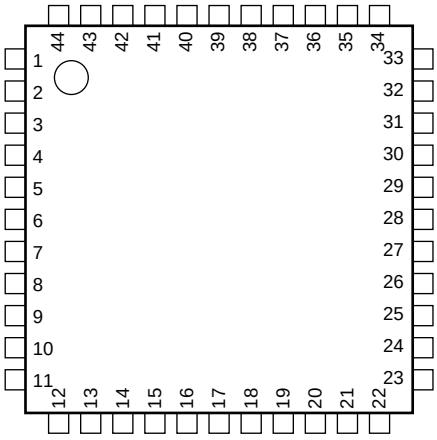
Pin No.	Symbol	I/O	Function
16~19,22~26	A0~A10	I	Address Input
14	RAS	I	Row Address Strobe
28	CASH	I	Column Address Strobe/Upper Byte Control
29	CASL	I	Column Address Strobe/Lower Byte Control
13	WE	I	Write Enable
27	OE	I	Output Enable
2~5,7~10,31~34,36~39	I/O0~I/O15	I/O	Data Input/ Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

3. Block diagram



■ M6759 (U3) : MTP microcontroller

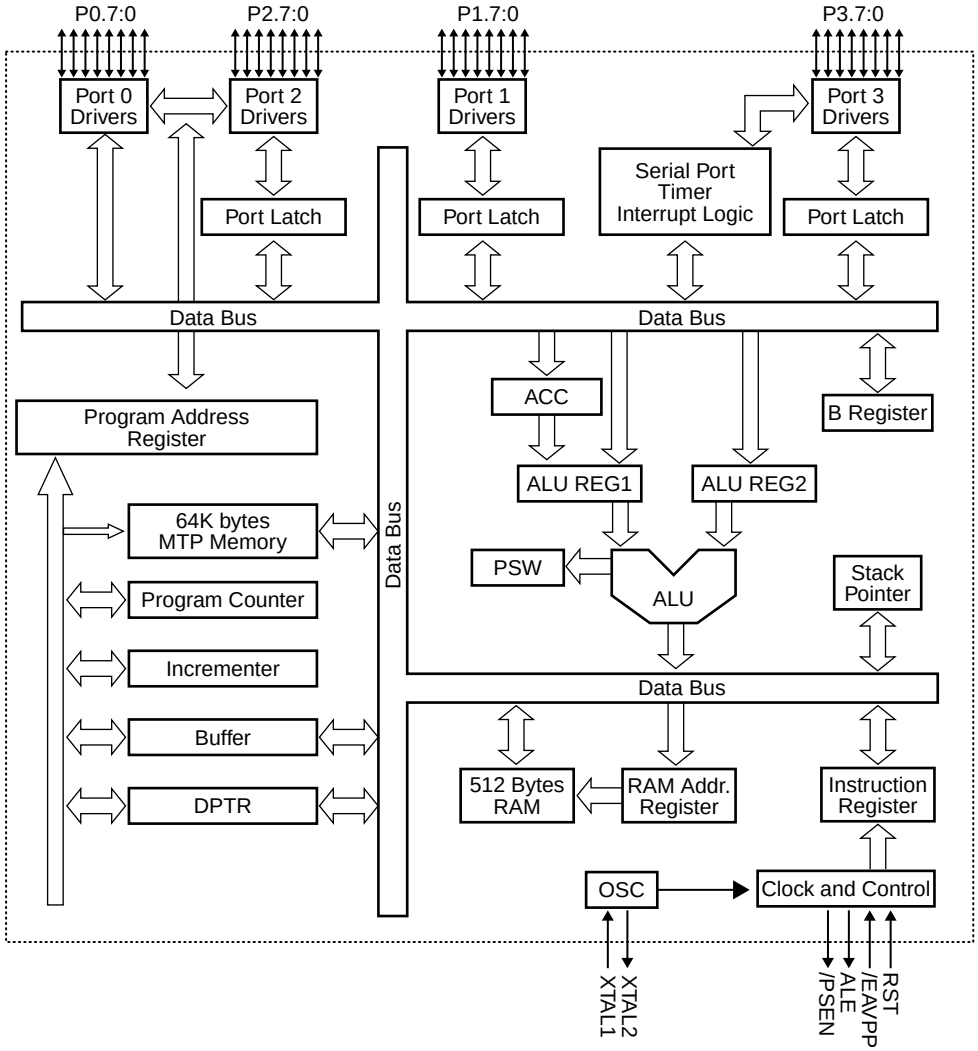
1. Pin layout



2. Pin function

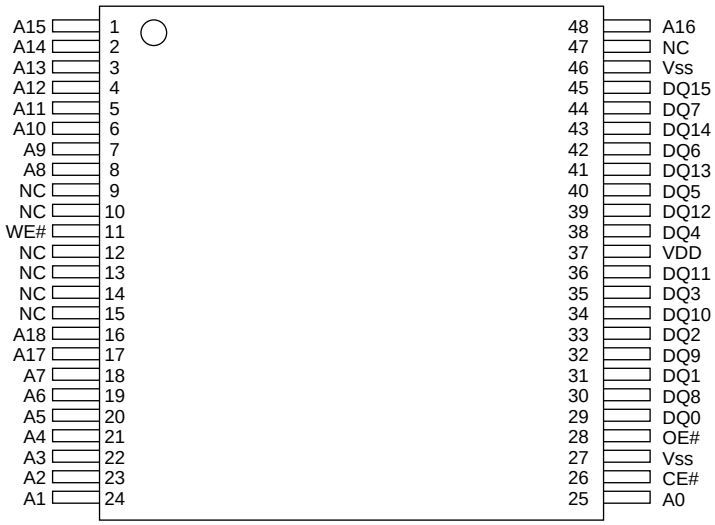
Pin No.	Symbol	I/O	Description
44	VDD	I	Power supply for internal operation, 5V input
22	GND	I	Ground
36,37,38,39,	P0.7-P0.0	I/O	8 bits bi-directional I/O port
40,41,42,43,	AD7-0	I/O	Multiplexed address/data bus
10	RST	I	Reset signal
21	XTAL1	I	Crystal In
20	XTAL2	O	Crystal out
32	/PSEN	O	Program Store Enable Output
33	ALE	O	Address Latch Enable
9,8,7,6,	P1.7-P1.0	I/O	8 bits bi-directional I/O port
5,4,3,2	T2EX(P1.1)	I	External timer/counter 2 trigger
	T2(P1.0)	I	External timer/counter 2.
31,30,29,28,	P2.7	I/O	8 bits bi-directional I/O port
27,26,25,24	A15-A8	O	
19,18,17,16,	P3.7-P3.0	I/O	8-bit bi-directional I/O port
15,14,13,11	/RD(P3.7)	O	External data memory read strobe
	/WR(P3.6)	O	External data memory write strobe
	T1(P3.5)	I	External timer/counter 1
	T0(P3.4)	I	External timer/counter .
	/INT1(P3.3)	I	External interrupt 1 (Negative Edge Detect)
	/INT0(P3.2)	I	External interrupt 0 (Negative Edge Detect)
	TXD(P3.1)	O	Serial port output
	RXD(P3.0)	I	Serial port input
35	/EAVPP	I	
1,12,23,34	NC	-	

3. Block diagram

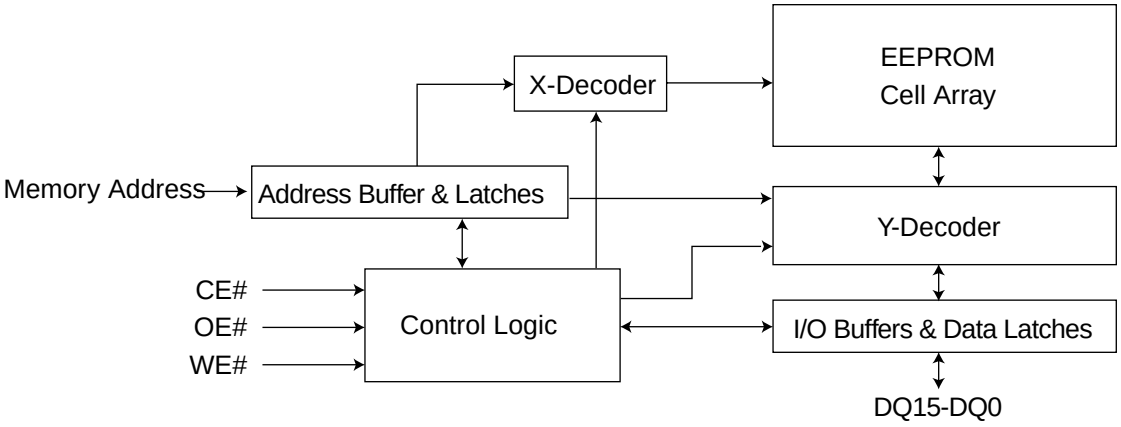


■ SST39VF800A (U6) : 8M Flash memory

1. Pin layout



2. Block diagram

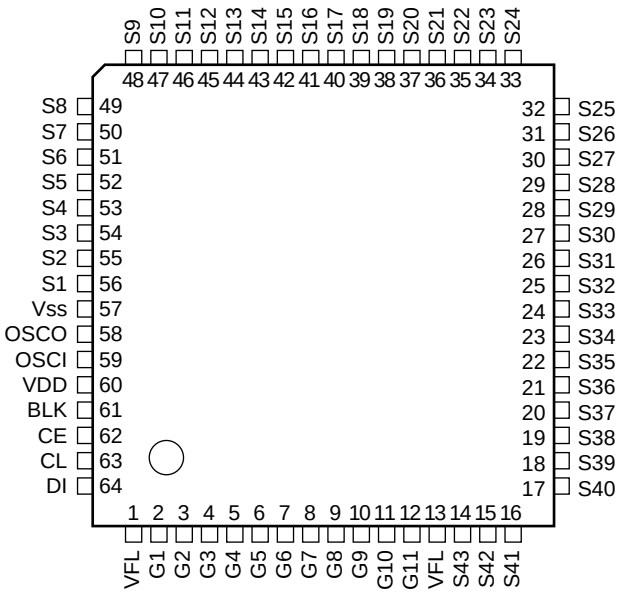


3. Pin function

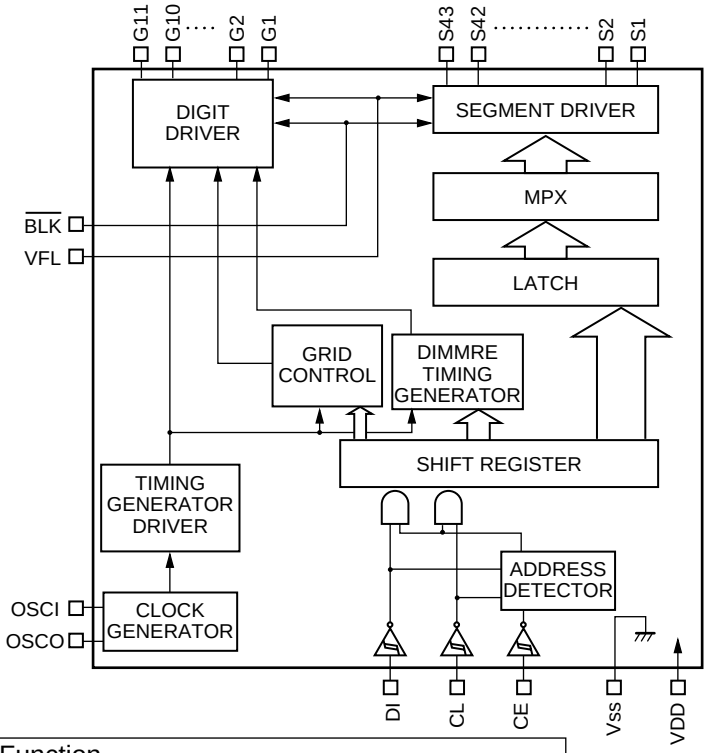
Symbol	Pin name	Function
AMS- A0	Address Inputs	To provide memory addresses. During Sector-Erase AMS-A11 address lines will select the sector. During Block-Erase AMS-A15 address lines will select the block.
DQ15- DQ0	Data Input/Output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
VDD	Power Supply	To provide power supply voltage: 2.7-3.6V
Vss	Ground	
NC	No Connection	Unconnected pins.

■ LC75725E (UIC10) : VFD driver

1. Pin layout



2. Block diagram

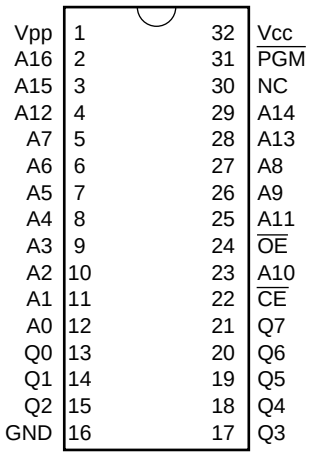


3. Pin function

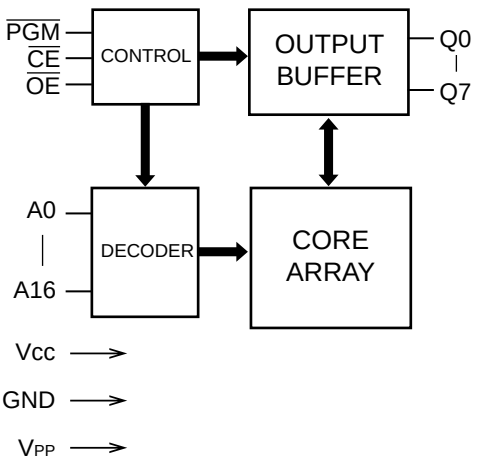
Pin No.	Symbol	I/O	Function
1,13	VFL	-	Driver block power supply connection. (Both pins must be connected.)
60	VDD	-	Logic block power supply connection. Provide a voltage between 4.5 and 5.5V.
57	Vss	-	Power supply connection. Connect to the ground.
59	OSCI	I	Oscillator connection. An oscillator circuit is formed by connecting an external resistor
58	OSCO	O	and capacitor to these pins.
61	$\overline{BLK}$	I	Display off contort input. BLK = Low (Vss)...Display off.(S1 toS43 and G1 to G11 at VFL level.) BLK = High (VDD)...Display on. Note that serial data can be transferred while the display is turned off.
63	CL	I	Serial data transfer inputs. These pins must be connected to the system microcontroller.
64	DI		CL: Synchronization clock
62	CE		DI: Transfer data CE: Chip enable
2-12	G1-G11	O	Digit outputs. These pins are P-channel open drain outputs with pull-down resistors.
56-14	S1-S43	O	Segment outputs for displaying the display data transferred by serial data input. These pin are P-channel open drain outputs with pull-down resistors.

■ W27L010 (DIC21) : EPROM

1. Pin layout



2. Block diagram

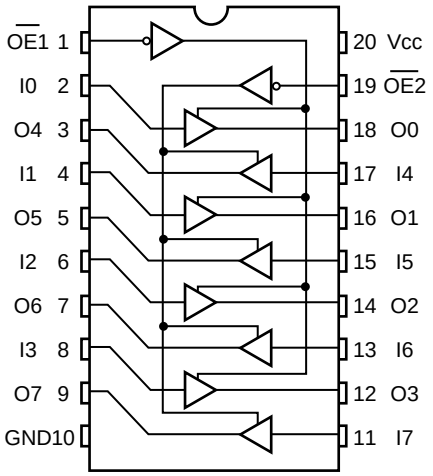


3. Pin function

Symbol	Function
A0~A16	Address Inputs
Q0~Q7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
V_{PP}	Program/Erase Supply Voltage
Vcc	Power Supply
GND	Ground
NC	No connection

■ 74VHCT244A (DIC12) : Buffer/Line driver

1. Pin layout



2. Pin function

Symbol	Function
$\overline{OE1}$,$\overline{OE2}$	3-STATE Output Enable Inputs
I0-I7	Inputs
O0-O7	3-STATE Outputs

3. Truth table

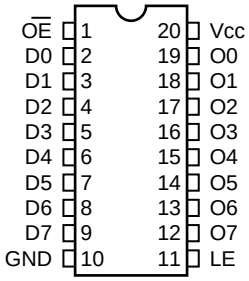
Inputs		Outputs (Pins12,14,16,18)
$\overline{OE1}$	In	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins3,5,7,9)
$\overline{OE2}$	In	
L	L	L
L	H	H
H	X	Z

H:HIGH Voltage Level
L:LOW Voltage Level
I:Immaterial
Z:High Impedance

■ 74LVT573 (U10, U11, U12) : Latch

1. Pin layout



2. Pin function

Symbol	Function
D0-D7	Data Inputs
LE	Latch Enable Input
OE	Output Enable Input
O0-O7	3-STATE Latch Outputs

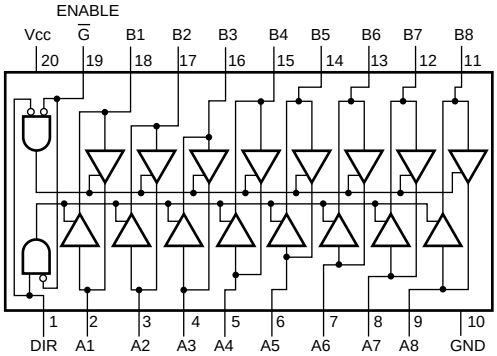
3. Truth table

Inputs			Outputs
LE	OE	Dn	On
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O0

H:HIGH Voltage Level
L:LOW Voltage Level
Z:High Impedance
X:Immaterial
O0:Previous O0 before HIGH to LOW transition of Latch Enable

■ MM74HCT245 (U15) : Transceiver

1. Pin layout



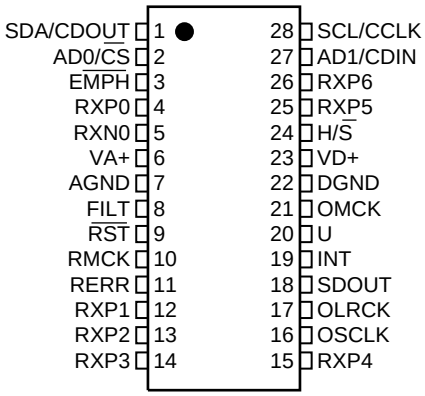
2. Truth table

Control Inputs		Operation
$\overline{G}$	DIR	245
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H=HIGH Level
L=LOW Level
X=Irrelevant

■ CS8415A (DIC14) : Digital audio receiver

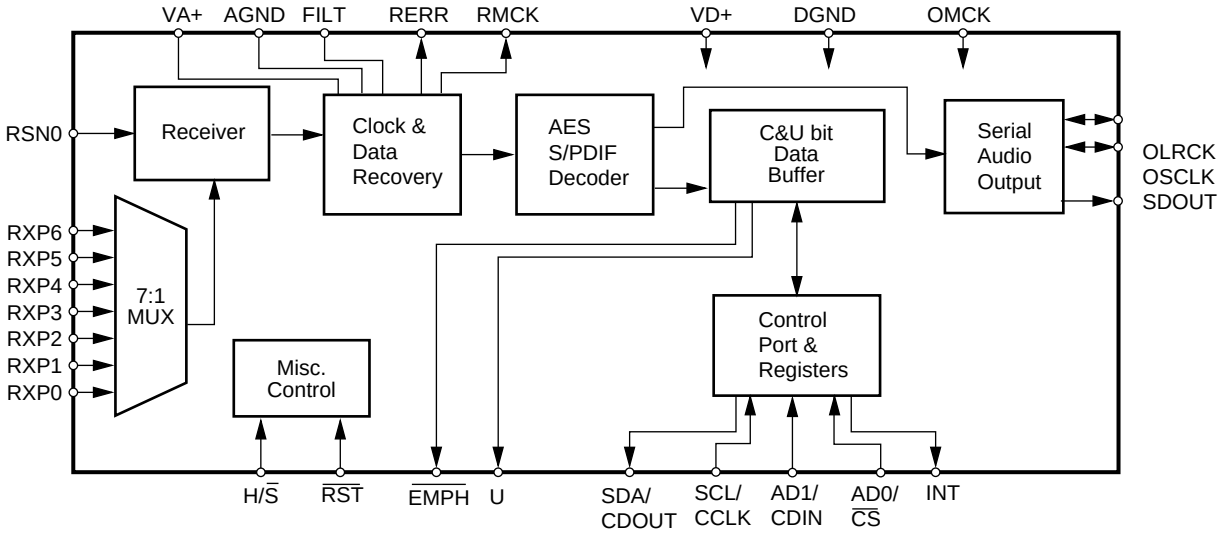
1. Pin layout



2. Pin function

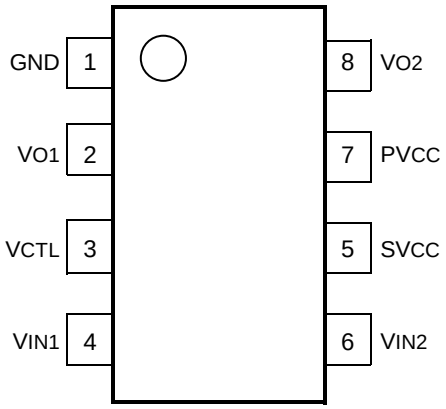
Pin No.	Symbol	I/O	Function
1	SDA/CDOUT	I/O	Serial Control Data I/O(I2C) / Data Out(SPI)
2	AD0/$\overline{CS}$	I/O	Address Bit 0(I2C) / Control Port Chip Select(SPI)
3	$\overline{EMPH}$	O	Pre-Emphasis
4 5	RXP0 RXN0	I	AES3/SPDIF Receiver Power
6	VA+	I	Positive Analog Power
7	AGND	I	Analog Ground
8	FILT	O	PLL Loop Filter
9	$\overline{RST}$	O	Reset
10	RMCK	I/O	Input Section Recovered Master Clock
11	RERR	O	Receiver Error
12,13 14,15 25,26	RXP1,RXP2 RXP3,RXP4 RXP5,RXP6	I	Additional AES3/SPDIF Receiver Port
16	OSCLK	I/O	Serial Audio Output Bit Clock
17	OLRCK	I/O	Serial Audio Output Left/Right Clock
18	SDOUT	O	Serial Audio Output Data
19	INT	O	Interrupt
20	U	O	User Data
21	OMCK	I	System Clock
22	DGND	I	Digital Ground
23	VD+	I	Positive Digital Power
24	H/$\overline{S}$	I	Hardware/Sofrware Mode Control
27	AD1/CDIN	I	Address Bit 1(I2C) / serial Control Data in (SPI)
28	SCL/CCLK	I	Control Port Clock

3. Block diagram

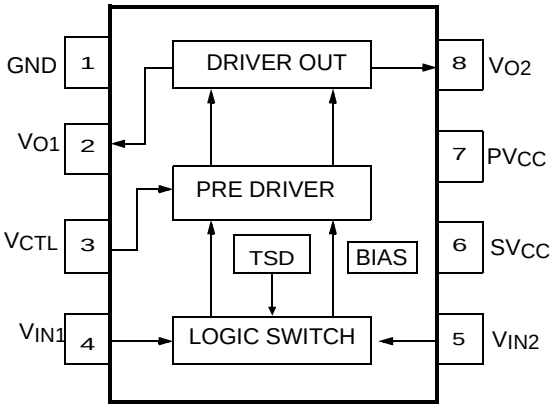


■ FAN8082 (U10) : DC motor driver

1.Pin layout



2. Block diagram

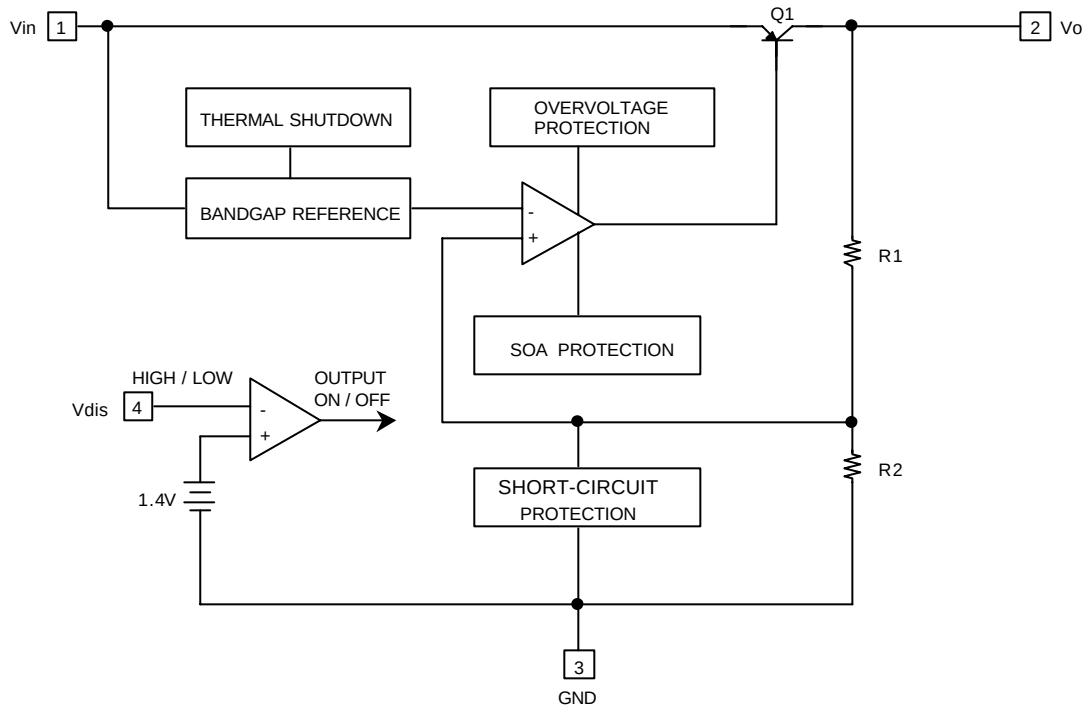


3. Pin function

Pin No.	Symbol	I/O	Function
1	GND	-	Ground
2	V_{O1}	O	Output 1
3	V_{CTL}	I	Motor speed control
4	V_{IN1}	I	Input 1
5	V_{IN2}	I	Input 2
6	SV_{CC}	-	Supply voltage (Signal)
7	PV_{CC}	-	Supply voltage (Power)
8	V_{O2}	O	Output 2

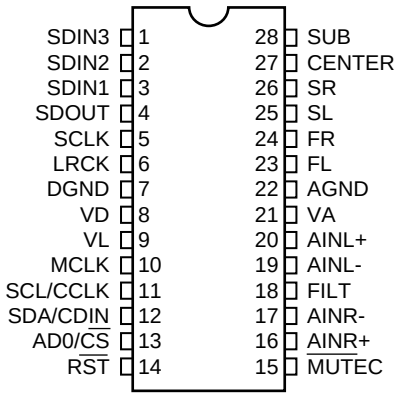
■ KA78R05 (PQ2,PQ6)/ KA78R08 (PQ5)/ KA278R05 (PQ1)/ KA278R33 (PQ4) : Regulator

1. Block diagram



■ CS4228A (DIC15) : D/A converter

1. Pin layout

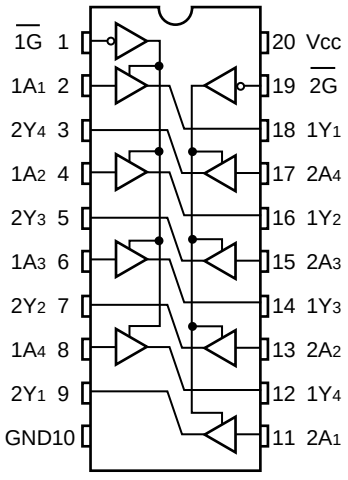


2. Pin function

Pin No.	Symbol	Function
1,2,3	SDIN1 SDIN2 SDIN3	Serial Audio Data In
4	SDOUT	Serial Audio Data Out
5	SCLK	Serial Clock
6	LRCK	Left/Right Clock
7	DGND	Digital Ground
8	VD	Digital Power
9	VL	Digital Interface Power
10	MCLK	Master Clock
11	SCL/CCLK	Serial Control Interface Clock
12	SDA/CDIN	Serial Control Data I/O
13	ADO/$\overline{CS}$	Address Bit 0/ Chip Select
14	$\overline{RST}$	Reset
15	MUTEC	Mute Control
16,17 19,20	AINR+,AINR- AINL+,AINL-	Differential Analog Inputs
18	FILT	Internal Voltage Filter
21	VA	Analog Power
22	AGND	Analog Ground
23,24,25 26,27,28	FR,FL,SR,SL SUB,CENTER	Analog Outputs

■ 74LCX244 (DIC13) : Bus buffer

1. Pin layout



2. Pin function

Pin No.	Symbol	Function
1	$\overline{1G}$	Output Enable Input
2,4,6,8	1A1 to 1A4	Data Inputs
9,7,5,3	2Y1 to 2Y4	Data Outputs
11,13,15 17	2A1 to 2A4	Data Inputs
18,16,14 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Outputs Enable Input
10	GND	Ground(0V)
20	Vcc	Positive Supply Voltage

3. Truth table

INPUT		OUTPUT
$\overline{G}$	An	Yn
L	L	L
L	H	H
H	X	Z

X:"H"or"L"
Z:High impedance

VICTOR COMPANY OF JAPAN, LIMITED
AUDIO & COMMUNICATION BUSINESS DIVISION
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